DESIGN OF A SENSITIVE, LOW-NOISE CMOS IMAGE SENSOR FOR
DIAGNOSING DIABETIC RETINOPATHY

by

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Abstract

Diabetic Retinopathy is a complication of Diabetes Mellitus and leads to vision loss and blindness. With early detection and diagnosis, the risk of severe vision loss can be prevented or mitigated. Diabetic Retinopathy is characterized by abnormal blood vessels in the retina and is currently only diagnosed by eye specialists in an invasive procedure where a fluorescent dye is injected into the bloodstream and the blood vessels in the eye are imaged over time. However, patient compliance with recommended eye specialist visits is low. Working towards developing an instrument that can be used by the primary care physician to perform a preliminary diagnosis would greatly increase early detection of this disease.

Laser speckle contrast imaging (LSCI) is a wide-field optical imaging technique that can measure blood flow non-invasively and is thus an excellent candidate to diagnose Diabetic Retinopathy non-invasively by looking at blood vessel size, location and health. However, for retinal imaging, the illumination must be low to avoid damaging the eye, and the result is low quality images in commercial complementary metal-oxide semiconductor (CMOS) image sensors. While charge-coupled device (CCD) cameras provide superior image quality, they require cooling for low noise images, resulting in a bulky, expensive device that is not suited for use by a primary care physician.

In this work, a custom designed CMOS image sensor was designed to acquire high quality images in low light conditions. Based on safe illumination levels and constraints of LSCI, the design of the sensor was optimized for high sensitivity and low noise at every stage from selection of technology, photodiode structure, pixel design and analog-to-digital (ADC) design.

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Chapter 1: Clinical Background

Section 1.1: Diabetic Retinopathy

Section 1.1.1: Prevalence

Today an estimated 382 million people are affected by Diabetes Mellitus, more commonly known as Diabetes [1]. Among patients who have Diabetes Mellitus, 35% of them have Diabetic Retinopathy [1]. In 2004, 4.1 million U.S. adults over 40 had Diabetic Retinopathy [2]. Diabetic Retinopathy is a complication of Diabetes Mellitus that can lead to blindness. It is the leading cause of blindness in middle-aged adults in developed countries [1] and also the leading cause of blindness in the United States for patients aged 20-74 [3]. Early treatment and therefore early detection is very effective in preventing and mitigating the effects of Diabetic Retinopathy. Patients who were not screened promptly after being diagnosed with type 2 Diabetes had a higher rate of Diabetic Retinopathy compared to patients who were screened promptly after being diagnosed [4]. It was also shown that with early detection, the risk of severe vision loss can be reduced by more than 90% [3].

Section 1.1.2: Classification

Diabetic Retinopathy can be broadly classified into two categories: Non-proliferative Diabetic Retinopathy (NPDR) and Proliferative Diabetic Retinopathy (PDR). Within NPDR, it can be further classified as mild to moderate, severe, or very severe. Mild to moderate is diagnosed by microaneurysms and intra-retinal hemorrhages in the retina, mostly in the posterior pole [1]. This leads to the breakdown of the blood brain barrier, plasma leaks in retinal capillaries, and retinal edema [1]. Ultimately this leads to vision loss or vision distortion. 20-25% of patients who develop Macular edemas develop vision loss within 10 years [1].

Severe NPDR is diagnosed when any of the following three conditions occur: intra-retinal hemorrhages in all four quadrants, venous beading in two quadrants, or intra-retinal microvascular abnormalities in one quadrant [1]. Very severe NPDR is diagnosed when two of the severe conditions are present [1].
Proliferative Diabetic Retinopathy (PDR) is diagnosed when new, fragile retinal vessels grow from the retinal capillaries into the vitreous [1]. These new vessels can break and cause pre-retinal and vitreous hemorrhages, which lead to floaters and vision loss [1]. As vessels grow over the vitreous, glial and fibroblast cells form epiretinal membranes that induce traction retinal detachment [1]. Sometimes neovascular growth can cause neovascular glaucoma [1].

Section 1.1.3: Treatments

There are multiple treatments available for Diabetic Retinopathy, and they can be categorized into four methods: Systemic Factor Control, Laser Therapy, Pharmacotherapy, and Surgical Therapies. Systemic factor control is further split up into regulating glucose, blood pressure, cholesterol and anemia.

A number of studies were done on the relationship between glucose level control and the development and management of Diabetic Retinopathy. In one study where type one Diabetes participants’ glycated hemoglobin levels were less than 6% (or 42.1mmol/mol), the progression of existing Diabetic Retinopathy was decreased by 54% and the prevention of the development of Diabetic Retinopathy increased by 76% [5]. In another study where the median glycated hemoglobin level was 7% (or 53mmol/mol) versus 7.9% in the control, there was a decrease of 25% for the rate of microvascular disease for type two diabetics [6]. In a third study, tight control of glucose of 6.4% versus 7.5% in the control led to a reduced progression of Diabetic Retinopathy by 35% in four years [7]. However, a Meta study showed that intensive control of blood glucose did not prevent severe vision [8].

Controlling blood pressure also seems to decrease the incidence of Diabetic Retinopathy. In the UKPDS study, controlling blood pressure was found to lead to a decrease in visual loss [6]. In the ACCORD-Eye study, they found that tight blood pressure control did not significantly decrease the incidence of Diabetic Retinopathy; there was a therapeutic threshold around 130mmHg systolic [7]. A third study found that treating high blood pressure with Cardesartan led to a 25% decrease in the development of Diabetic Retinopathy for patients with type one diabetes, and a 34% decrease for patients with type 2 diabetes [9].

There was also a link found between cholesterol levels and the development of Diabetic Retinopathy. One study found that LDL and TG were directly related to the incidence and severity of
Diabetic Retinopathy [10]. Another study found that Fenofibrate, a drug used to treat high cholesterol, reduced the need for laser treatment for Diabetic Retinopathy in type two diabetics [11]. In the ACCORD-Eye study, they found that Fenofibrate used with Simvastatin (another drug used to treat high cholesterol) in type two diabetics slowed the progression of Diabetic Retinopathy [7]. Similarly, one study has associated Anemia with the progression of Diabetic Retinopathy [12] [13]. These studies suggest that controlling Diabetes will help prevent the development of Diabetic Retinopathy or at least slow it down.

Another treatment option patients have is Laser Therapy. In one treatment, small, light intensity burns can be applied to the microaneurysms to help reduce vision loss by 50% [14]. A second method is to use a sub-thermal intensity laser applied to retinal pigment epithelial (RPE) cells in order to reduce damage to the functional retinal tissue and reduce deep burns [1]. It uses longer laser wavelengths (647nm or 810nm) and micropulsar techniques to reduce unnecessary damage to the eye [1]. A third method is to use a horse-shoe shaped macular grid to simultaneously apply laser photocoagulation (cauterizing blood vessels using laser) over a preset pattern [1]. Pan-retinal photocoagulation, or scatter photocoagulation, reduced the risk of severe vision loss by 50% over five years [15]. It is a method to slow the growth of new blood vessels by using multiple laser burns.

Diabetic Retinopathy can also be treated with the administration of drugs, or Pharmacotherapy. The first class of drugs used is anti-VEGF drugs. High VEGF levels in the vitreous for patients with Diabetes affect endothelial tight junction proteins and phosphorylate molecules that break down the blood brain barrier [1]. Current VEGF drugs include aptamer, pegptanib, monoclonal antibody fragment Ranibizumab, bevacizumab, VEGF-Trap, siRNAs, bevasiranib, rapamycin, which are injected into the eye [1]. The second class of drugs is steroids, which are used to decrease inflammation; inflammation can eventually lead to alteration of the blood brain barrier [1].

Finally, Diabetic Retinopathy can be treated using more invasive surgical therapies such as Vitrectomy surgery if needed [1].
Section 1.2: Constraints Imposed by Imaging the Eye

We are interested in imaging the microvasculature of the eye. The size of microvasculature in the eye varies from 100 microns to 300 microns for the diameter of the vessels [16]. This requires that the camera including the optics must be able to resolve these sizes.

The main constraint from the eye is the amount of light that we can input into the eye. Light can damage the eye in three ways. The first way is Photomechanical damage, which occurs when a rapid input of energy causes tissue damage from tensile and compressive forces caused by the shockwave [17]. This forms microcavitation bubbles, which kill RPE cells [17]. This type of damage is determined from the rate of delivery of energy, and the amount of energy [17]. The second way is Photothermal damage where thermal lesions form when the temperature is raised by more than 10 degrees Celsius than the ambient temperature of the retina [17]. The third way is photochemical damage when electrons get excited and split bonds to produce reactive oxygen species; these free radicals attack molecules, breaking down membrane structures [17]. Blue light causes severe retinal damage (green light causes no damage), and the amount of damage is directly related to the strength of illumination [17].

Photochemical damage can be classified as class I or class II damage. In class I, the action spectrum is the same as the absorption spectrum for visual pigment, and the exposure is hours to weeks of exposure to low irradiances (below 1mW/cm²) [17]. Most of the damage for class I occurs to the photoreceptors [20]. In class II, the action spectrum peaks at short wavelengths, and the exposure is to high irradiances of white light (above 10mW/cm²); the initial damage for class II is to the pigment epithelium [17].

Photochemical damage in humans is usually caused by two sources: the sun or optical instruments. Macular lesions can occur from viewing solar eclipses [17]. The RPE cells are usually damaged directly, but they regenerate rapidly [17]. However, photoreceptors degenerate and disappear sometime after the exposure [17]. It is thought that blue light alone causes the damage [17]. Latrogenic Exposure to light or damage from ophthalmic instruments can occur from operating microscopes and endoillumination during Vitrectomy surgery [17]. Chronic degeneration can occur months to years after the initial injury [17].
Light exposure can also affect Age-related Macular degeneration (AMD). It has been found that long exposure to visible light predisposes the eye to AMD, and exposure to sunlight is correlated with AMD [17].

Section 1.3: Need For Screening at Primary Care

Currently, Diabetic Retinopathy is only diagnosed by eye specialists. Upon being diagnosed with Diabetes Mellitus, primary care physicians refer the patient to an eye specialist for yearly examinations [18]. The examinations are done by an ophthalmologist or optometrist [19]. It is recommended that patients 10 and older with type 1 diabetes should have a comprehensive eye exam within five years after being diagnosed [19]. Type two diabetics are recommended to have a comprehensive eye exam shortly after being diagnosed [19]. It should be noted that high quality fundus photography interpreted by a trained eye care provider is not considered a substitute for a comprehensive eye exam [19].

The comprehensive eye exam usually comprises of six parts. First, the examination starts with a visual acuity test [20]. Secondly, the eye specialist will then examine the eyes using an Ophthalmoscope and slit lamp [20]. Thirdly, if glaucoma is suspected, then a Gonioscopy is done [20]. Fourthly, Tonometry is done to measure the pressure inside the eye [20]. Next, the eye specialist uses special imaging modalities to look at the blood vessels [20]. Optical Coherence Tomography is done to look at the cross-section of the retina, and finally a Fluorescein Angiogram is done to look at blood flow [20].

Although the comprehensive eye exam is effective in diagnosing patients, many patients do not actually get their eye exams done frequently enough. For patients under Medicare, it was found that a little over 50% had at least a 15 month gap between eye exams within the first 30 months of being diagnosed with Diabetic Mellitus [21]. For patients under private healthcare, only 16% had annual eye exams in a two year period [21]. It has also been found that geography and the distance from an eye care facility has an effect on compliance. Patients living more than 8 miles from an eye care facility were found to be less likely to be compliant [21].

Thus, one solution is to have some form of screening at the primary care level. Patients usually have frequent visits to their primary doctor, at least once a year. A device that primary physicians can use with little training to quickly do a preliminary diagnoses of Diabetic Retinopathy would not only raise
awareness of Diabetic Retinopathy, but it would also encourage patients who are suspected to have Diabetic Retinopathy to go get a comprehensive examination.
Chapter 2: State of the Art

Section 2.1: Imaging Techniques

Section 2.1.1: Positron Emission Tomography (PET scan):

This technique involves injection or inhalation of a radiopharmaceutical [22]. The radiopharmaceuticals are biological compounds that emit positrons. After injection, there is usually a short wait time of seconds to minutes before imaging begins [22]. Usually the positron will annihilate when it collides with an electron after traveling a small distance, emitting two photons in opposite directions [22]. If the photodetector senses two photons in a short time period, then this means a positron was emitted [22].

It is then possible to estimate the amount of radiopharmaceuticals at different locations in the body [22]. This technique can be used to calculate various biological metrics including blood flow, glucose metabolism and receptor binding characteristics [22]. There are two major disadvantages to this technique. The first is the requirement of an on-site cyclotron in order to generate the radiopharmaceuticals since they decay quickly [22]. This makes the cost of this imaging modality high. The second is the requirement of introducing the radiopharmaceuticals to the body, either through injection or inhalation meaning that this technique is invasive.

Section 2.1.2: Magnetic Resonance Imaging:

Magnetic Resonance Imaging is a technique that takes advantage of the property that particles can have an intrinsic angular momentum or spin [23]. These particles absorb RF energy in a narrow frequency band whose frequency depends on the strength of the magnetic field [23]. A gradient of magnetic field is applied along a slice so that along the gradient, the frequency of emission is different [24]. Then a broadband RF signal is applied, and the resulting signal of different frequencies of emissions is acquired over time [24]. This is then Fourier transformed and the signal at each frequency, which corresponds to different locations in the scan, can be acquired [24]. To get a 2D image, this process can be repeated multiple times with a rotating gradient field [24]. The result measures the proton concentration at different locations in the scan, and it has been shown that different tissues have different proton concentrations [24].
Among non-invasive Magnetic Resonance Imaging techniques, functional Magnetic Resonance Imaging (fMRI) can be used to visualize microvasculature [25]. Paramagnetic Deoxyhemoglobin is a natural MRI contrast agent that occurs in venous blood [25]. The resulting contrast in the image is dependent on the level of blood oxygenation [25]. This technique can be used to image veins in tissue.

Another technique called phase contrast MRI allows flow velocities to be calculated. A bipolar magnetic field gradient is applied [26]. This is a gradient which goes in one direction for a certain time, then goes in the opposite direction for the same amount of time [26]. The bipolar magnetic field gradient has no net effect on stationary spins, but it does have a net effect on flowing spins [26]. By subtracting the phases from the different parts of the bipolar gradient, it is possible to calculate a velocity vector [26]. By doing this for multiple gradient directions, a 3D velocity vector field can be calculated [26].

Although MRI is a very powerful imaging technique that can visualize vessels and measure flow, it is not applicable because the high cost of a MRI machine makes it unfit for primary care.

**Section 2.1.3: Vascular Casting:**

Vascular Casting is a way to visualize microvasculature in extreme detail, but it involves sacrificing tissue. First the blood is replace with saline or ringer’s solution at the appropriate blood pressure [27], then the tissue is infused with resin until it polymerizes [27]. The tissue is removed using maceration, leaving casts of the vasculature [27]. The vasculature can then be imaged in detail, usually with a scanning electron microscope for high resolution images of the vasculature [27]. Obviously this technique cannot be used here because it involves sacrificing the tissue.

**Section 2.1.4: Fluorescence Imaging:**

Two types of fluorescence imaging are used for blood flow imaging in the retina: Fluorescein Angiography and Indocyanine Green Angiography. The two techniques are very similar, but use different fluorescent dyes. The procedure and concept of operation is the same for both. First the dye is injected intravenously [28]. The dye is excited by light and fluoresces, emitting light at a specific wavelength [28]. The light is then filtered to block excitatory light and captured using an imaging modality [28]. During this process, the eye is usually dilated to let more light enter and exit the eye [28], and the eye is continuously imaged for a period of 15-20 minutes after injection [28]. Flow can be measured by looking at the speed the
dye enters the vessels in the eye. A Scanning Laser Ophthalmoscope can be used to acquire the image for an ultra-wide field of view (up to 200 degrees) [29]. Compared to Fluorescein, Indocyanine Green has a longer wavelength, resulting in better penetration for imaging deep ocular structures [29]. This is better for imaging choroidal vasculature, especially age-related macular degeneration (AMD) [29]. The main downside to using fluorescence imaging is that it requires the injection of dye into the patient. It also takes some time (around 20 minutes) to acquire images, and requires someone that is knowledgeable in eye pathologies to interpret [28].

Figure 2.1: Fluorescein Angiography. The top left image shows a fundus image of the eye while the top right and bottom images show different stages of Fluorescein Angiography [30].
Figure 2.2: Indocyanine Green Angiography and OCT. A and B are IGA images with A being an image acquired early in the process and B an image acquired late in the process. C is a B-scan of the same eye using OCT [29].

Section 2.1.5:  Confocal Microscopy:

Confocal microscopy is usually used to image fixed tissue which is labeled with fluorescent probes [31]. The tissue is scanned using a beam of light (usually a laser); this eliminates out of focus light because only the light from the fluorescence in the focal plane is emitting light [31]. In other words, when the specimen is scanned, most of the scattering in a pixel is from the incident light for that pixel, but when the whole specimen is lit, most of the scattering is not from light incident for that pixel [31]. By eliminating out of focus light that is present when using wide view microscopy, the resolution improves. To speed up the process, multiple beams can be used at once. A Confocal Scanning Laser Ophthalmoscope (SLO) is the application of confocal microscopy to image the eye. Scanning can be done using two mirrors: one for vertical scan and one for horizontal [31]. This technique is invasive, since it requires fluorescence.
Section 2.1.6: Two (Multi) Photon Microscopy (2PLSM):

Two photon microscopy allows for even greater resolution than confocal microscopy by using non-linear methods [33]. Like confocal microscopy, this technique reduces out of focus light further and uses fluorescence. For a two photon microscope, a molecule needs excitation from two photons that arrive almost simultaneously (within a window of about 0.5 fs) in order to bump it up an energy level into an excited state where it can fluoresce [33]. This method requires very high resolution in space and time by the excitatory light source [33]. Thus ultra-short laser pulses are needed (on the order of picoseconds), which
are very expensive [33]. While this technique offers high resolution, it requires fluorescence and an expensive laser to work.

**Figure 2.4:** A Jablonski diagram showing the energy levels of the fluorescence molecules in a Two Photon Microscopy set up [33]. Note how it requires two photons in order to reach the excited state.

**Section 2.1.7: Laser Speckle Contrast Imaging:**

When a coherent light source hits a randomly scattering medium, the light that comes back to the photodetector will form speckles, or interference patterns [34]. The speckles have the property of being random in space and intensity, forming a speckle pattern [34]. When this is applied to a region with blood flow, the moving particles will cause fluctuations in the interference pattern, which is detected by the photodetector as fluctuations in intensity [34]. Looking at the statistics in the temporal or spatial domain (or a mix of both), it is possible to obtain 2D images of blood flow [34].

Moving particles create a blur in the acquired image, which corresponds to a lower standard deviation from the mean. For calculation of LSCI, the K map is first computed where the K value at each
pixel is given by equation (2.1), where I is the intensity; the standard deviation and mean are calculated for a group of pixels (usually 7x7 array) or for a single pixel over many frames (usually 80 frames) [34].

\[ K = \frac{\sigma}{\langle I \rangle} \]  

(2.1)

The tau map can be calculated using equation (2.2) where T is the exposure time and \( \frac{T}{\tau} \) is proportional to flow velocity [35].

\[ K^2 = \frac{T}{2T} \left[ 2 - \frac{T}{T} \left( 1 - \exp\left( -\frac{2T}{\tau} \right) \right) \right] \]  

(2.2)

The spatial resolution of this technique is around 10 microns, and the temporal resolution is from about 10ms to 10 seconds [35]. The main advantage of this technique is that it is a wide field technique that does not require scanning while having high resolution [34]. This means faster acquisition times.

**Section 2.1.8: Optical Coherence Tomography:**

Optical Coherence Tomography (OCT) is an optical imaging technique useful for imaging deeper into the tissue for in vivo imaging [36]. This optical technique is commonly used to image deep eye structures, and it can penetrate distances exceeding 2 cm [37]. It requires either a low coherent light source or a laser that can generate very short pulses; low coherence light can generate resolutions around 10 microns while pulsed lasers can generate resolutions up to 1 micron [38]. There are three general requirements for the light source: it should emit near IR in order to image deep structures, it should have a short coherence length to get higher resolution and contrast, and it should have high irradiance in order to capture weak backscattering structures in deep tissue [37].

The general principle behind the time domain OCT is as follows: emitted light is split into a reference signal and a sample signal [36]. The sample signal goes to the sample and the light that comes back is scattered by the biological tissue [36]. The reference light is usually reflected off a mirror, and the reference and sample signals are recombined [36]. Because a low coherence light source is used, the output only appears when the phase of the signal and reference are close [36]. The amplitude is proportional to the scattering properties of the tissue [36]. The reference mirror is moved back and forth (using a stepper motor) to change the phase of the reference in order to image at different depths in the tissue (longitudinal
scanning) and create what are called A-scans (axial) [36]. B-scans are created by doing multiple A-scans at
different lateral locations [36].

It is possible to measure the blood flow in the tissue using what is called Doppler Optical
Coherence Tomography (DOCT), which can be done in the time or frequency domain [39].

In time domain DOCT, the reference arm is shifted at a constant velocity v_{ref}. The heterodyne frequency is
given by equation (2.3) where \( \lambda \) is the central wavelength. With a Doppler shift \( f_D \), the modulation frequency is now given
by equation (2.4) where \( v_s \) is the velocity of flow, \( \alpha \) is the angle between the illumination direction and
velocity vector, and \( n \) is the refractive index of the surrounding medium [39].

\[
f_{het} = \frac{2v_{ref}}{\lambda} \quad (2.3)
\]

\[
f = f_{het} + f_D \cdot v_s = \frac{f_D \lambda}{2n \cos(\alpha)} \quad (2.4)
\]

The full fringe signal can be recorded using the time domain OCT described above, and then the
local frequency shift in a window that can be slid across the A-scans can give an idea of flow [39].
However, this technique cannot capture flow in the smaller vessels in the retina since the flow rate is too
slow [39].

In the Frequency domain, Fourier Domain Optical Coherence Tomography (FDOCT) can achieve
higher speed and sensitivity compared to the time domain DOCT [39]. In this method, the spectral
interference pattern can be recorded using what is called spectrometer based FDOCT or using a swept
source OCT where the reference arm is fixed instead of being moved by a stepper motor [39]. Spectrometer
based FDOCT uses a spectrometer to record the interference pattern in parallel while swept source OCT
uses a wavelength-tuning source to acquire the interferogram as a function of time [39].

Using FDOCT, it is possible to measure the phase change between two adjacent A-scans, and
calculate the velocity using equation (2.5) where \( T \) is the time between the two scan and \( \Delta \varphi(X, Z) \) is the
change in phase [39].
\[ v(X, Z) = \frac{\lambda \Delta \varphi(X, Z)}{4n\pi T} \] (2.5)

**Figure 2.5** A basic OCT set up. In this set up the SLD is a super luminescent diode acting as the light source, the PZT is a piezoelectric transducer that introduces phase shift to the signal from the sample, and the reference is shifted back and forth to do longitudinal scanning. The light recombines after it is reflected from the sample and reference; with a low coherent light source, when the time delay from the light path is matched, the signal is higher compared to when it is mismatched [36].

In summary, OCT is a powerful imaging method for imaging deep biological structures in vivo as well as to measure flow in the tissue. However, the time domain method requires an accurate stepper motor while FDOCT requires a spectrometer or wavelength-tuning source.

**Section 2.1.9: Laser Doppler Flowmetry:**

Laser Doppler Flowmetry uses coherent laser illumination and detects the frequency shift between moving red blood cells and static tissue [40]. This imaging modality normally utilizes scanning, but it can be applied as a wide-field technique [41]. Using a PMT or avalanche photodiode, the power of the photocurrent is a function of the frequency shift (Doppler shift power spectrum), so the velocity of blood flow can be measured [40]. As I will discuss in the section about avalanche photodiodes, these detectors are currently not widely used in large arrays. However it can also be imaged using a regular CMOS sensor [41].
Section 2.1.10: Optical (Reflectance) Microscopy:

Optical Microscopy or wide field microscopy measures visible light that scatters to the detector with magnifying optics. As the magnification goes up, the contrast decreases, so there is a trade-off between magnification and contrast in this method [42]. Furthermore, this technique does not directly measure flow, but it only measures the different scattering of tissue.

In order to summarize different imaging techniques, a table on the next page has been included of the imaging techniques discussed above.
### Table 2.1: Imaging Techniques

<table>
<thead>
<tr>
<th>Imaging Technique</th>
<th>Invasive</th>
<th>Resolution</th>
<th>Field of View</th>
<th>Measures flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positron Emission Tomography</td>
<td>Yes</td>
<td>1mm [43]</td>
<td>Wide</td>
<td>Yes</td>
</tr>
<tr>
<td>Magnetic Resonance Imaging</td>
<td>No, unless used with contrast agents</td>
<td>100um [43]</td>
<td>Wide</td>
<td>Yes</td>
</tr>
<tr>
<td>Vascular Casting</td>
<td>Yes</td>
<td>1nm [43]</td>
<td>Scanning</td>
<td>No</td>
</tr>
<tr>
<td>Fluorescence Imaging (IGA, FA)</td>
<td>Yes</td>
<td>Hundreds of microns [43]</td>
<td>Wide</td>
<td>Yes</td>
</tr>
<tr>
<td>Confocal Microscopy (with fluorescence)</td>
<td>Yes</td>
<td>200nm [43]</td>
<td>Scanning</td>
<td>Yes</td>
</tr>
<tr>
<td>Two (Multi) Photon Microscopy (with fluorescence)</td>
<td>Yes</td>
<td>50nm [44]</td>
<td>Scanning</td>
<td>Yes</td>
</tr>
<tr>
<td>Laser Speckle Contrast Imaging</td>
<td>No</td>
<td>10 microns [35]</td>
<td>Wide</td>
<td>Yes</td>
</tr>
<tr>
<td>Optical Coherence Tomography</td>
<td>No</td>
<td>10 microns [43]</td>
<td>Scanning</td>
<td>Yes</td>
</tr>
<tr>
<td>Laser Doppler Flowmetry</td>
<td>No</td>
<td>Millimeters [41]</td>
<td>Scanning or Wide</td>
<td>Yes</td>
</tr>
<tr>
<td>Optical (Reflectance) Microscopy</td>
<td>No</td>
<td>Diffraction Limited (limited to about 200 microns)</td>
<td>Wide</td>
<td>No</td>
</tr>
</tbody>
</table>
Ideally, a non-invasive imaging method would be better for a primary care setting. Furthermore, a wide field technique is preferred over a scanning technique because of faster acquisition times and lower cost (due to need for less precise instruments). Next, measuring flow is also important for classifying vessels. Finally a sub-100 micron resolution is needed to capture the microvasculature. With these constraints, only Laser Speckle Contrast Imaging remains. LSCI is also a cheap technology since it only requires a coherent light source (laser diode) and a CMOS camera, which lends itself to use in primary care.

**Section 2.2: Camera Image Sensors**

Among camera sensors, the two widely used types of sensors today are charge coupled devices (CCD) and complementary metal oxide semiconductors image sensors (CIS). Each has their own advantages and disadvantages, which will be discussed below.

**Section 2.2.1: Charge-Coupled Devices:**

CCD cameras are sensors that collect and transfer charge [45]. Each pixel usually contains three polysilicon gates [45]. The gate with the higher voltage within the pixel collects all the charges under it [45]. The camera sensor is exposed to light, which generates charges within the pixel with quantum efficiencies up to 90% (if special techniques are used) [45].
During the light collection or integration stage, the gate of A has a high voltage (see Figure 2.6), so all the charges will collect under A. The charge can then be transferred in three stages. In the first stage the voltage at the gate of B increases while the voltage at the gate of A decreases; this transfers the charge from under A to B [45]. In the second stage, the same process is done, and the charge is transferred from B to C [38]. Finally in the third stage, the charge is transferred from C to A of the next pixel [45]. This process is repeated until all charges are read off of the pixel array. At the end of the array, the signal is measured by converting the charge to a voltage or a current [45].

Section 2.2.2: Complementary Metal Oxide Semiconductor (CIS):

CIS use standard CMOS technology [45]. Because of this, they have the advantage of being cheaper, and they have the ability to include active circuitry within the same die as the pixels. However, with the addition of circuitry, the fill factor is reduced (usually 50-70%), and fixed pattern noise is introduced [45]. CIS can use different types of photo sensors, which include photodiodes, photogates, phototransistors, and photoconductors [45].
Section 2.2.3: Photodetectors

Section 2.2.3.1: Photodiodes

Figure 2.7: A PN junction showing the creation of holes and electrons at the PN junction through diffusion.

Photodiodes are formed using a PN junction. A PN junction is made up of a P-doped material and an N-doped material. P-doping is when silicon is implanted with impurities that introduce electron acceptors such as Boron. N-doping is when silicon is implanted with impurities that introduce electron donors such as phosphorus.

When a photon absorbed by the semiconductor produces enough energy to transfer an electron from the valence to the conduction band, an electron-hole pair is generated [45]. If this happens far from the depletion region, they will likely recombine [45]. However, if they occur in the depletion region or near enough to diffuse into the depletion region before combining, the electric field will sweep the electrons and holes, leading to a photocurrent [45]. Thus a larger depletion region leads to more photocurrent [45].
depletion region is affected by the electric field, so applying an external voltage to the diode can change the depletion region size [45]. Increasing \( V_N - V_P \) or reverse biasing the diode increases the depletion region size while increasing \( V_N - V_P \) or forward biasing the diode decreases the depletion region size [45]. Forward biasing pushes holes in the p region and electrons in the n region towards the junction, reducing the depletion region. Reverse biasing increases the depletion region size. Electrons and holes can diffuse into the depletion region and be swept across, producing a current or voltage [45]. Quantum efficiency of a photodiode can be increased by making the depletion region thicker, but this also makes it slower [45]. One way to make the depletion layer thicker is to introduce a layer of semiconductor between the p and n junctions, forming a PIN diode [45]. Because there is a strong electric field at the depletion region, photodiodes are much faster than a photoconductor [45].

The speed of a photodiode is determined by diffusion time of the carriers outside of the depletion layer, drift time inside the depletion layer, and the time constant from the load resistance and parasitic capacitance [45]. Putting the junction near the surface reduces the diffusion time outside of the depletion layer [45]. Strongly reverse biasing the diode reduces drift time inside the depletion layer and also reduces parasitic capacitances [45].

**Section: 2.2.3.2: Photogates:**

Photogates consist of a MOS capacitor with a piece of polysilicon as the top terminal [45]. It is closely related to a CCD, and its operation is the same [45]. First the voltage on the gate over the p-substrate is pulsed high, pushing holes away from the surface, forming a depletion layer near the surface [45]. This attracts photo-generated electrons under the gate [45]. This method integrates charge rather than voltage or current. However, because it must transfer charges, there is an additional noise source from transfer noise [45].
Section: 2.2.3.3: Phototransistors:

Phototransistors are usually implemented using Bipolar Junction Transistors rather than MOS transistors because they usually have better responsivity due to the current flowing through a larger volume [45]. A large base junction, which is left floating, collects photons, and the holes formed are swept into the collector as a collector current [45]. This increases the emitter-base potential, and more holes from

Figure 2.8: A Photogate is shown. Vr is pulsed high to integrate charge [45].

Figure 2.9: A PNP phototransistor. The large collector-base junction area is to increase the number of photons collected [45].
the emitter go into the base, further increasing collector current [45]. Phototransistors can provide gain while sensing, but there is a tradeoff between high gain and low noise; phototransistors are also slow compared to photodiodes [45].

**Section: 2.2.3.4: Photoconductors**

Finally, photoconductors are semiconductors with ohmic contacts at their ends [45]. As photons are absorbed, the conductivity of the semiconductor increases [45]. Photoconductors can have very high gain up to 1000, but they are slow and have high noise [45].

---

**Figure 2.10:** The photoconductor structure is shown in (a) and a typical bias circuit for the photoconductor is shown in (b) [45].

---

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Table 2.2: Comparison of Photodetectors

<table>
<thead>
<tr>
<th>Type</th>
<th>Compatible with CMOS Technology</th>
<th>Noise</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photodiode</td>
<td>Yes</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Photogate</td>
<td>Yes</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Photoconductor</td>
<td>No, (resistor process variation)</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Phototransistor</td>
<td>No</td>
<td>High</td>
<td>High</td>
</tr>
</tbody>
</table>

Photodiodes and Photogates are both possible choices for photodetectors in a pixel array used in a CMOS Process. A CMOS compatible structure would be preferable because of lower cost. Additionally, photogates cost more transistors to implement in an active pixel design because of the need to pulse the photogate and transfer the charges (5 vs. 3 in a minimal structure) [45].

Section 2.2.4: Pixel Structures

CMOS cameras can have two types of pixels: active pixels or passive pixels. Active pixels provide gain within the pixel and buffer the pixel to reduce the capacitance of each pixel as well as lower read noise, improve dynamic range and improve the signal to noise ratio [45]. However, the cost is a lower fill factor and fixed pattern noise [45].

Section 2.2.4.1: Photodiode APS

One of the common active pixels is the photodiode APS (Active Pixel Structure). This pixel has three transistors: a reset transistor, a row select transistor for readout, and a source-follower transistor to buffer the pixel [45]. Its operation is as follows: the reset transistor is switched on, which charges the photodiode capacitor to the supply voltage. During the phototransduction stage, the photodiode capacitor is discharged for the exposure time; the amount discharged is proportional to the incident light. A source-follower transistor buffers the capacitor voltage. When it is time to read out the value, the row select transistor turns on, which exposes the buffered capacitor voltage to the column bus. Usually a correlated double sampling circuit is used in every column to reduce fixed pattern noise [45].
**Figure 2.11:** Photodiode APS showing the classic 3-pixel design. M1 resets the voltage on the photodiode, M2 acts as a source follower and M3 selects the pixel when it is being read out [45].

Photodiode APS is commonly used as a part of larger pixel design. Yamaguchi et al. designed a self-reset CMOS image sensor to be implanted into a mouse brain to measure hemodynamic responses [46] [47]. The APS pixel feeds into a Schmitt trigger which triggers a reset of the pixel when enough light has fallen on it. By doing this, the pixel can have high sensitivity over a high dynamic range, allowing the sensor to get a high maximum SNR.

**Figure 2.12:** Self-reset CMOS pixel design featuring an APS architecture combined with a Schmitt Trigger [47].
Section: 2.2.4.2: Photogate APS

Another pixel structure is the photogate APS. While the charge is being integrated by the photogate, the output is reset and the reset value is read by a sample and hold circuit in the CDS (Correlated Double Sampling). A pulse signal then transfers the charge from the photogate to a source follower, where the result is then read by a second sample and hold circuit in the CDS. This is usually a 5 transistor circuit (Reset transistor, row select, source follower, TX, Photogate) [45].

![Photogate APS](image)

**Figure 2.13:** Photogate APS featuring a 5 transistor design. PG stands for photogate and tells it when to integrate charges, TX transfers the charge to the rest of the pixel, SF stands for source follower and RS stands for row select [45].

Section: 2.2.4.3: Pinned Photodiode APS

The Pinned Photodiode APS uses a pinned diode (p+-n-p) so photons are collected away from the surface because surface defects produce noise [45]. During readout, this charge is transferred to an output floating diffusion [45]. This design is similar to a photogate, but it requires 4 transistors instead of 5 (doesn’t need a photogate pulse). Thus it has a higher fill factor than the photogate APS, but it has a small full well capacity because of the pinned photodiode and a lower Quantum Efficiency [45].
Figure 2.14: Pinned Photodiode APS: TX transfers the charge to the rest of the pixel, Reset sets the voltage of the photodiode to vdd, SF acts as a source follower and RS selects the pixel for readout [45].

Section: 2.2.4.4: Logarithmic Photodiode APS

The logarithmic Photodiode APS is another three transistor pixel circuit. However, this pixel does not need a reset and runs continuously [45]. The voltage at the photodiode is about equal to the supply voltage. The load transistor above is in the subthreshold region; thus the voltage at the photodiode is given the equation below, where $I_0$ is a lumped constant term.

$$V_{PH} = V_{DD} - \Delta V_{PH} = V_{DD} - \frac{KT}{q} \ln \left( \frac{I_{PH}}{I_0} \right) [45]$$

Additionally there is a buffer and a row select transistor. However this circuit has several major disadvantages: it is very temperature dependent, has low swing at the output for low light levels, and high fixed pattern noise [45].
Figure 2.15: Logarithmic Photodiode APS. IDS is the subthreshold current going through the transistor and is equal to $I_{ph}$ [45].

In one design by Guo, a normal APS architecture was combined with a logarithmic architecture to provide high dynamic range [48]. The pixel would initially operate as a normal APS pixel; however, when a certain voltage level is exceeded, a shared OTA between the linear and log circuits triggers a control signal which switches the pixel into logarithmic mode by turning on the branch connected to VDD.

Figure 2.16: Linear and Logarithmic pixel structure schematic [48].
Section: 2.2.4.5: Capacitive Transimpedance Amplifier APS (CTIA APS)

In this type of pixel structure, reset puts the photodiode voltage to the DC operating point of the inverting amplifier (Figure 2.17) [49]. $C_{fb}$ (feedback capacitor) is much smaller than the $C_{pd}$ (photodiode capacitance). Writing KCL at the input of the amplifier in the Laplace domain yields:

$$I_{pd}(s) + \left(\frac{v_{out}(s)}{A} - v_{out}(s)\right) sC_{fb} + \frac{v_{out}(s)}{A} s C_{pd} = 0$$  \hspace{1cm} (2.7)

Solving for $v_{out}(s)$:

$$v_{out}(s) = \frac{I_{pd}(s)}{sC_{fb} \left(1 - \left(1 + \frac{C_{pd}}{C_{fb}}\right) \frac{1}{A}\right)}$$  \hspace{1cm} (2.8)

Assuming the gain $A$ is very high, that is $A \gg \frac{C_{pd}}{C_{fb}} > 1$, then

$$v_{out} \approx \frac{1}{C_{fb}} \int I_{pd} dt \quad [49]$$  \hspace{1cm} (2.9)

Thus this structure integrates the charge onto the feedback capacitor instead of the photodiode capacitance, which allows more control over sensitivity and more accurate capacitance values [49]. It also allows the selection of photodiode size and photodiode capacitance to be independent [50].
Figure 2.17: CTIA pixel structure. C_{fb} is a feedback capacitor that is smaller than the photodiode capacitance [49].

Section: 2.2.4.6: Digital Pixel Sensor

A digital pixel design incorporates the ADC into each pixel, resulting in a parallel readout [51]. This allows for very fast readout and thus is useful for very high resolution imagers [51]. The ADC used is an integrating ADC; the ramp generation and counter can be shared among all pixels, and within each pixel is an op-amp that compares whether the value of the ramp has exceeded the pixel value [51]. When the value is exceeded, the register within each pixel will latch the counter value [51]. This method also has the advantage of low capacitive load on the pixels, resulting in lower noise. However, this structure has low fill factor and has quantization noise from the ADC (not useful for very sensitive measurements with a small pixel size) [52].
Spivak et al. implemented a sensitive Digital Pixel sensor in a larger 30µm pixel [53]. The main advantage of this architecture is that after the signal is digitized, there is essentially no noise, so digitizing it earlier reduces noise sources.

**Figure 2.19:** Pixel Design of a pixel with an open loop amplifier to digitize the signal right away [53].
Section: 2.2.4.7: DC Level Mode APS

In DC Level Mode APS, the average intensity level is used (including the reset value) [44]. Usually the signal $\nu$ is given by equation (2.10) where $v_2$ is the reset level and $v_1$ is the intensity level at the end of integration [44]. However, if we take the output given by equation (2.11) instead, the SNR goes up. This is because the reset level is related to the light signal as well so it provides more information [52]. Deen et al. showed that the DC level (or reset level) at low light levels ($1\mu W/cm^2$) had an SNR about 20 dB better than the swing [52].

$$\nu = v_2 - v_1 \quad (2.10)$$

$$\nu = \frac{v_1 + v_2}{2} \quad (2.11)$$

Section: 2.2.4.8: Single Photon Avalanche Photodiodes

Single Photon Avalanche Photodiodes allows the detection of single photons in light starved imaging applications. Single Photon Avalanche Diodes (SPAD) act like PMTs when operated in Geiger mode [52]. They can be made using a p+/n-well diode biased near its breakdown voltage [52]. Placing a guard ring using an n-well placed within the p+ region spreads the breakdown region over the diode instead of just at the edges [52].

Once the diode starts breaking down, it must be quenched in order to stop conduction so that it can sense the next photon [54]. A passive resistor is added as seen in Figure 2.21 to add passive quenching [54]. When the Avalanche Photodiode (APD) starts breaking down, current will flow through the passive resistor [54]. This makes the excess bias drop out and stops breakdown [54]. The voltage then charges back up to the initial bias in the reset phase [54]. An RC constant during breakdown mode (quenching) and re-charge mode (resetting) is the result of the resistor [54]. Active quenching can also be done where a transistor can turn on to speed up quenching or resetting [54]. A common architecture for this is to have an NMOS that turns on after some time of passive quenching, quickly draining the node near ground; after another delay the NMOS is turned off, and a PMOS is turned on to quickly restore the voltage at the SPAD [54]. The output is a count of the number of spikes, so a counter must be implemented in each pixel [54].
Although SPADs are very sensitive and fast (don’t require long integration times), they have lots of circuitry in each pixel. In the implementation shown in Figure 2.20 was done in a 130nm CMOS process; the pixel size was 32x50 microns, and the fill factor was only 6% [54].

![Figure 2.20: schematic of the pixel of an Avalanche photodiode circuit [54].](image)

![Figure 2.21: Avalanche Photodiode with active and passive quenching [54].](image)
Section: 2.2.4.9: Asynchronous Image Sensors

Asynchronous Image Sensors contain fully autonomous pixels [55]. Each pixel decides when to reset and accesses the readout line only when it needs to [55]. In this Asynchronous Time-Based Image Sensor (ATIS) design, the goal is to do lossless compression by avoiding redundant data [55]. The output is only read out if it changes, and the pixel is only reset when a large enough change is detected in that pixel [55]. When an event occurs, digital pulses are generated where the time between digital pulses represents the light intensity [55]. Naturally, asynchronous image sensors can integrate for long periods of time when a reset is not needed, possibly increasing SNR.

Figure 2.22: Asynchronous Image Sensor that uses a change detector to decide when to reset [55]. (a) shows the pixel, (b) shows the timing diagram, (c) shows the change detector in the pixel, and (d) shows the waveforms in the change detector [55].
The change detector detects a change in the photodiode current with either ON events if the change is positive (increase) or OFF events if the change is negative (see Figure 2.22d) [56]. When an ON or OFF event occurs, Rst_B resets the photodiode voltage Vint to VDD where it decreases as it integrates the photodiode current (Figure 2.22b) [56]. Once it reaches VrefH, the comparator toggles, causes a pulse for Req_B[H], signaling the start of an acquisition [56]. The comparator reference is then switched to vref, and when Vint reaches vref, the comparator input goes high, causing a pulse for Req_B[L] [56]. This signals the end of acquisition and the output is tint1, which is the time between Req_B[H] and Req_B[L] [56]. This is inversely proportional to the average photocurrent during that time [56].

Section: 2.2.4.10: Charge, Current and Voltage Mode Pixel (APS)

The structures discussed above can be classified as Charge Mode Pixels, Current Mode Pixels, or Voltage Mode Pixels. Charge mode pixels integrate charge onto a capacitance. Current mode pixels take the photodiode current as the output, but it usually needs to be buffered when it is read out [45]. A voltage mode pixel is similar to a current mode pixel, but it uses a linear resistor to convert the current to a voltage signal [45].

![Figure 2.23](image196x183 to 452x388.png)

**Figure 2.23:** This shows the three different types of APS designs. (a) is a charge-mode pixel, (b) is a current-mode pixel (no reset), and (c) is a voltage-mode pixel (no reset) [45].
Section: 2.2.4.11: Passive Pixels

Passive pixels have the highest fill factor for CMOS image sensors and consequently also have the highest Quantum efficiency [45]. Each pixel has a photodiode and one transistor used as a charge gate [45]. When the transistor closes, the photodiode is reset, and the amount of charge used to reset the photodiode is equal to the amount of charge the photodiode discharged [45]. This is integrated onto a Charge Integration Amplifier (CIA); depending on the design, there may be one CIA for the whole array or one per column [38]. Passive pixel structures suffer from high capacitive loads, which make readout slow, noise high and create fixed pattern noise [45].

![Passive pixel structure diagram](image)

**Figure 2.24:** Passive pixel structure only having one transistor for row select [52].

This structure is used in CMOS image sensor that is used as a Fluorometer [57] [58]. In this design, the imager was designed to look at phase in order to resolve fluorescence events. With a small array of 32x32, the passive pixels share the readout circuitry, which consists of trans-impedance amplifier stage, comparator stage, and Time-to-Digital converter stage.
Section: 2.2.4.12: Comparison of Pixel Structures, Low Light Applications

Table 2.3: Comparison of Pixel Structures

<table>
<thead>
<tr>
<th>Pixel Structure</th>
<th>Number of Transistors</th>
<th>Sensitivity</th>
<th>Noise</th>
<th>Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photodiode APS</td>
<td>3</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Moderate</td>
</tr>
<tr>
<td>Photogate APS</td>
<td>5</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Moderate</td>
</tr>
<tr>
<td>Pinned Photodiode APS</td>
<td>4</td>
<td>Moderate</td>
<td>Low noise (avoids surface defects)</td>
<td>Low</td>
</tr>
<tr>
<td>Logarithmic Photodiode APS</td>
<td>3</td>
<td>Moderate</td>
<td>Temperature dependent output, high Fixed Pattern Noise</td>
<td>High</td>
</tr>
<tr>
<td>CTIA APS</td>
<td>5 [49]</td>
<td>High</td>
<td>Low dark current noise, most linear output [50]</td>
<td>Low</td>
</tr>
<tr>
<td>Digital Pixel Sensor</td>
<td>37 (8-bit) [51]</td>
<td>Adjustable</td>
<td>Low readout noise [50]</td>
<td></td>
</tr>
<tr>
<td>DC level Mode APS</td>
<td>3</td>
<td>Moderate</td>
<td>Lower than Photodiode APS relative to signal (including reset adds signal, increasing SNR)</td>
<td>Moderate</td>
</tr>
<tr>
<td>SPAD</td>
<td>30+ (not explicitly mentioned)</td>
<td>High</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Asynchronous</td>
<td>89 [56]</td>
<td>Adjustable</td>
<td>1.6nA/cm^2 dark noise, min. SNR 42.3dB [55]</td>
<td>Very High</td>
</tr>
<tr>
<td>Passive Pixel</td>
<td>1</td>
<td>Moderate</td>
<td>High</td>
<td>Moderate</td>
</tr>
</tbody>
</table>

For low light level applications, shot noise from the light source dominates. Thus, in order to maximize the Signal to noise ratio (SNR), the fill factor should be maximized to maximize the incoming
light, and the noise should be minimized. The signal also needs to be sufficiently large, which will require high sensitivity. Although a sufficient dynamic range is important, it is not a limiting factor in most designs in low light conditions.

The most commonly used pixel structure is the photodiode APS because it maximizes fill factor for an active pixel design, which has large advantages over passive pixels in terms of speed and noise. Digital pixel sensor, SPAD and asynchronous all have many transistors in the design, which doesn’t work well because a low fill factor is low, resulting in low SNR. Asynchronous design can get around this by integrating for longer even with a smaller fill factor to get sufficient light, but with LSCI, which is exposure time sensitive, a fully asynchronous pixel would not work well.

Logarithmic Photodiode APS has higher dynamic range compared to the Photodiode APS, but this is not important in low light applications. However, the cost of higher noise and temperature dependent makes the Photodiode APS a better choice.

Pinned Photodiode APS and DC level Mode APS both perform better than the Photodiode APS, so they are both viable options. The CTIA APS is also a good option because it has low dark noise and high sensitivity. The CTIA APS has higher noise than the Photodiode APS because of $1/f$ noise from the additional transistors [50]. However, in order to get the needed sensitivity, the Photodiode APS would need an amplifier stage after, which would introduce the same if not more $1/f$ noise (this is also true of Pinned Photodiode APS and DC level Mode APS). Thus, CTIA APS is the best balance in terms of high sensitive and low noise and is the structure that will be used.

Looking past the basic pixel design, the pixel can be further modified by either combining different basic designs or using a design for multiple pixels. Seo et al. implemented a photodiode APS where four photodiodes shared one read out structure (see Figure 2.25) [59]. The advantage of doing this is an increase in fill factor (this design had 1.75 transistors per pixel) with a cost in output capacitance at the photodiode [59]. It would also be possible to implement a pinned photodiode APS with other structures. For example, a pinned photodiode can be used in place of a photodiode and be used in any structures that use photodiodes.
Figure 2.25: Shared pixel design where four pinned photodiodes share the 3-transistor active pixel structure [59].

Section 2.2.5: CIS Readout Structures:

Section 2.2.5.1: Shutter Type:

To read out the data in a CIS, either a rolling shutter or a global shutter approach is used. In the rolling shutter approach, all pixels in a row are reset at once and are read out in parallel [45]. When a column is being read out, the signal value from one pixel is read out and then reset. The new reset is then compared to the signal value for CDS (correlated double sampling), which reduces fixed pattern noise [45]. In the global shutter approach, the integration time for all pixels in the array is the same. While the pixels are being read out, exposure is stopped; as a result the signal must be stored [45]. Each pixel thus has a
sample and hold capacitor; however, signal can be lost in the sample and hold stage through shutter leakage and limited storage capacitance [45].

**Section: 2.2.5.2: Digital Readout Structures:**

In digital readout structures where an on-chip ADC digitizes the signal before being read off, it can either be digitized by one ADC in the chip (Pixel by pixel or PBP), one ADC per column (Per-Column ADC or PC-ADC), or one ADC per pixel (Per-Pixel ADC or PP-ADC) [51]. PBP has the lowest fixed pattern noise since the same ADC is used to digitize every pixel; however because the same ADC is used, PBP also has the lowest frame rate (FR) given in equation (2.12) where $\tau_{ADC}$ is the time it takes for the ADC to digitize one pixel, H is the number of rows, V is the number of columns, b is the number of bits, n is the number of parallel outputs, and $\tau_{RO}$ is the time it takes the I/O to send the digital data [51].

For a PC-ADC, there is either one ADC per column or two ADC per column (one on top and one on the bottom of the column) [51]. This architecture has higher FPN than PBP and also a higher frame rate given by equation (2.13).

PP-ADC is the Digital Pixel Sensor described in previous sections and has even higher FPN due to a different amplifier every pixel, but it also has a higher frame rate due to parallel analog to digital conversion [51]. The frame rate is given by equation (4.22).

$$FR = \frac{1}{H \cdot V (\tau_{ADC} \frac{n}{V} + \tau_{RO})} \quad [51]$$ (2.12)

$$FR = \frac{1}{H \cdot V (-\frac{\tau_{ADC}}{V} \frac{b}{n} \tau_{RO})} \quad [51]$$ (2.13)

$$FR = \frac{1}{\tau_{ADC} + H \cdot V \cdot \frac{b}{n} \tau_{RO}} \quad [51]$$ (2.14)

**Section: 2.2.5.3: Analog Readout Structures:**

For even faster readout, the data is not converted to a digital signal; rather it is read out as an analog signal which saves the time from the ADC [51]. Among these Analog Readout Architectures are Parallel Analog Channels, Analog Frame Memory Array, and In-Pixel Analog Memory Unit.
Parallel Analog Channels is simply having multiple channels where Analog Data can be read out [51]. This allows for speeds of up to 5000fps for a 256x256 array of pixels with 16 parallel channels [51].

Analog Frame Memory Array is where the frame is stored as an analog signal in an array during capture and then converted by the ADC into a digital signal later [51]. This removes the limitations of the speed of the ADC while still preserving a digital output [51].

In In-Pixel Analog Memory Units, the analog frame is stored within a capacitor in each pixel, which allows for global shutter with very fast frame rates as well as faster frame rates in general because the value does not need to be read to the analog array before the next frame [51]. This technique can allow for frame rates up to 1.25 billion frames per second for 8 frames [51].

![Possible frame rates achievable using different readout architectures](image)

**Figure 2.26:** Possible frame rates achievable using different readout architectures [51].

**Section 2.3: Column Parallel ADC Architectures**

For imager chip designs, on chip analog to digital converters (ADC) are often time-interleaved to digitize the large amount of data. That is, there are multiple ADCs on chip that digitize data in parallel in order to quickly digitize the large array of data from the pixel array. For a rolling shutter readout structure where pixel data from a whole row is read out at the same time, a column parallel ADC architecture is convenient. For column parallel ADCs, the circuit should be compact and low power because the area and power costs are multiplied by the number of columns. Thus flash, 2-step, or interpolating architectures will not be considered here because they all require a large number of comparators, which translates to higher
area and power. Common architectures for column ADCs include Single-slope Ramped ADC, Multi-Ramp Single-Slope ADC (MRSS), Sigma-Delta ADC, Successive Approximation (SAR) ADC, and pipelined ADC.

**Section 2.3.1: Single-slope Ramped ADC**

Single-slope Ramped ADC offers the most compact circuitry. A ramped reference signal is produced for all columns and is compared to the signal value as an analog value. A comparator in each column will switch when the ramped signal crosses the signal value. When it switches, it will latch the digital counter value. Thus this architecture only requires a single comparator and a few switches for every column. However, since it must count through every value, this architecture takes $2^n$ clock cycles where $n$ is the number of bits [60].

**Section 2.3.2: Multi-Ramp Single-Slope (MRSS) ADC**

Multi-Ramp Single-Slope (MRSS) ADC uses the same idea as the Single-Slope Ramped ADC. The difference is there are multiple ramps starting at different DC offsets in order to reduce the number of clock cycles needed. If there are $m$ ramps, then it will take $\frac{2^n}{m}$ clock cycles to digitize $n$ bits [61].

**Section 2.3.3: Sigma-Delta ADC**

The Sigma-Delta ADC oversamples the signal and then filters out the high frequency components later to achieve high resolution using a single comparator. This architecture has high resolution and low temporal noise. However, to achieve high resolution, the number of samples per bit increases. For a second order incremental sigma delta as implemented by Xhakoni et al. [62], the number of bits is given by equation (2.15) where $M$ is the number of clock cycles. For 10 bits, $M$ is approximately 45.

$$N = \log_2(M(M + 1)) - 1 \quad (2.15)$$

For a first order delta sigma converter, the signal-to-quantization-noise ratio (SQNR) is

$$SQNR = \frac{9M^2(\text{OSR})^3}{2\pi^2} \quad [63] \quad (2.16)$$
This equation assumes the $M$ is the peak amplitude of a full-scale input sine wave scaled by the quantization level, and OSR is the oversampling ratio. Using, the empirical SQNR limit for first order systems using 1-bit modulators, to achieve 10 bits requires an OSR of approximately 100 [63]. In the implementation of the second order delta sigma, the design required two comparators, two amplifiers, a digital to analog converter (DAC) implemented with switches, and digital filters [62]. For a first order delta sigma such as one implemented by Greenwald et al., one amplifier, one DAC, one comparator, and digital filters were required [64].

**Section 2.3.4: Successive Approximation ADC**

Successive Approximation ADCs require $n$ comparisons to digitize a signal into $n$ bits by using a binary search algorithm. There are two main types of Successive Approximation ADCs, cyclic or algorithmic ADCs and charge redistribution ADCs.

**Section: 2.3.4.1 Cyclic / Algorithmic ADC**

Cyclic or Algorithmic ADCs are fast and only require $n$ clock cycles to digitize a signal into $n$ bits. In the first stage, the signal value is sampled and held by a sample /hold circuit. The signal is roughly digitized in the second stage and the residue is fed back after being amplified [65]. This is done until the desired number of digital bits is acquired. Typically these are implemented to digitize 1.5 bits per cycle so that comparator offset only appears as an offset at the output instead of distorting the digitization. In terms of complexity, this architecture requires an amplifier for the sample / hold stage, an MDAC (Multiplying Digital to Analog Converter) to amplify and feedback the residue, a comparator, and digital logic [66].

**Section: 2.3.4.2 Charge Redistribution ADC**

Charge redistribution ADCs are low power because they rely on charge redistribution and require a single comparator, switches and a large capacitor array (usually binary weighted) [67]. In the first phase, the bottom terminals of the capacitors are connected to the input signal and the top terminals are connected to the common mode voltage of the comparator. In the second phase, a binary search algorithm is implemented by switching the voltage on the bottom plate of a given capacitor. For the MSB, the MSB
capacitor’s bottom plate is connected to Vref and the rest are connected to ground. The comparator is then comparing Vin-Vref/2 to ground. If the result is greater than zero, then the MSB capacitor and the next bit (MSB-1) are tied to Vref while the rest are tied to ground. If the result is less than zero, then the next bit is tied to Vref and all other capacitors are tied to ground. This is repeated n times where n is the number of bits. This type of ADC only requires a single comparator, an array of switches, binary weighted capacitors and digital logic to control the switches.

Section: 2.3.4.3 Pipelined ADC

Pipelined ADCs are similar to cyclic ADCs; except instead of feeding back the residue to the same amplifier, the residue is fed to the next amplifier in the pipeline [66]. For an n-bit pipeline ADC, there are n stages, so the ADC can start digitizing a new sample when the previous sample is still within the pipeline. This makes the architecture faster than Successive Approximation ADCs, but they consume more power and area.

Section 2.3.5: Hybrid Architectures

In recent image sensor chips, some column parallel ADC designs have employed a mixture of single slope ramp ADC and SAR/ Cyclic ADCs. Two stage Single Slope ADCs operate like single slope ramp ADCs; however, they first do a coarse level analog to digital conversion and then a fine level analog to digital conversion. After the coarse level analog to digital conversion, the residue is passed to the second stage where fine level analog to digital conversion is done. In an implementation by Lim, a DC offset determined by the coarse level analog to digital conversion is added to the fine level analog to digital conversion and the input signal is kept constant [68]. Teymouri’s implementation differs by using a differential current mode structure for the comparator to achieve smaller layout, lower power consumption and higher speeds [69]. Hassan recently made a multi-step version with variable number of steps, which allows for increased accuracy at the cost of time when desired [70]. Compared to SAR or cyclic structures, multi-step single slope ramp ADCs are simpler in the column because the DAC is shared across all columns, and they are also more accurate because the error does not compound across n cycles (n being the number of bits). As the number of cycles increase, the residue amplifier needs to become more and more accurate. Thus their speed and accuracy is between a single slope ramp ADC and SAR/ Cyclic ADCs.
Section 2.4: Noise

Section 2.4.1: Light Source Shot Noise:

The electrons generated by photons fluctuates according to a probability that is Poisson distributed [71]. This results in shot noise where the variance is given by equation (2.22).

\[ \sigma_e^2 = \mu_e \]  

Where \( \mu_e \) is the mean number of collected electrons [71]. This is given by quantum mechanics and is the same for all image sensors for a given light level hitting the photodetector [71].

Section 2.4.2: Shot Noise in Photodiodes

When current flows through a diode, carriers must cross a depletion region; the fluctuations that occur when they cross make up shot noise [72]. This can also be modeled as white Gaussian noise because it has a mean of zero and a wide and flat bandwidth [72]. A common model is a current source in parallel with the current through the diode [72] where the power spectral density is given by equation (4.22).

\[ S_i(f) = qi \]  

The DC current through the photodiode is \( i \), and \( q \) is the charge of an electron in coulombs [72].

Section 2.4.3: Flicker Noise Photodiode and MOS Transistors

Crystal defects and defects in electronics create traps which randomly trap and release carriers, causing fluctuations [72]. In Semiconductors, the flicker noise is proportional to the inverse of the frequency as given by equation (4.22).

\[ S_i(f) \propto \frac{1}{f} \]  

Section 2.4.4: Thermal Noise in MOS Transistors:

Thermal energy will occasionally move electrons in a resistive region of the transistor, causing fluctuations in current and voltage [72]. This noise has a mean of zero as well as a flat and wide bandwidth, so it can be modeled as white Gaussian noise [72]. During analysis, it can be modeled as a voltage source in series with a resistor, or a current source in parallel with a resistor [72]. The power spectral density for
the voltage source model is given by equation below where k is Boltzmann’s constant, T is temperature and R is the value of the resistor [72].

\[ S_p(f) = 2kTR \]  

\[ (2.20) \]

**Section 2.4.5: Dark Current**

Dark current is generated by thermally induced electrons and gives rise to a current when there is no light on the photodiode [71]. Dark current itself is subject to shot noise and flicker noise [72].

It is possible to reduce dark current through active means. Cheng et al. designed a photogate structure where the light is integrated twice for the same amount of time using different voltage biases at the photogate [73], thus the resulting output voltages are:

\[ \Delta V_1 = S_1 \ast L_x \ast t_c - V_{dark1} [73] \]  

\[ (2.21) \]

\[ \Delta V_2 = S_2 \ast L_x \ast t_c - V_{dark2} [73] \]  

\[ (2.22) \]

where \( S_1 \) and \( S_2 \) are the optical sensitivities under the different bias conditions, \( L_x \) is the illumination intensity, \( t_c \) is the reset cycle time and \( V_{dark} \) represents the voltage drop from dark noise [73]. \( V_{dark1} \) is approximately the same as \( V_{dark2} \) [73]. Dark current in this APS is mainly due to leakage currents occurring in the surface depletion region, which does not change much from changing the bias of the gate [73]. Thus subtracting the two signals cancels most of the dark current:

\[ V_o = \Delta V_2 - \Delta V_1 - (S_1 - S_2) \ast L_x \ast t_c \]  

\[ (2.23) \]
Chapter 3: Pixel Design

Section 3.1: Process Selection:

A capacitive trans-impedance amplifier design was used for the pixel design to achieve high sensitivity. The design was implemented in a 0.35µm process in order to use linear poly-poly capacitors which have lower capacitance per area compared to metal-insulator-metal capacitors as well as lower minimum capacitor area. This results in a smaller capacitor in the pixel, leading to higher sensitivity. Opto processes were not available for the chosen pixel size given our budget and the foundries that would work with us. Thus a standard CMOS process was chosen for this design.

Section 3.2: Pixel Specifications

The speckle size is given by equation (3.1).

\[
D = 2.44\lambda(1 + M)f_n [74]
\]  

(3.1)

D is the speckle size diameter, M is the optical magnification, \(\lambda\) is the wavelength, and \(f_n\) is the numerical aperture.

Kirkpatrick et. al found that the best laser speckle images occurred when the speckle size was approximately twice the size of the pixel [74]. In previous work done by Rege, a wavelength around 632nm was optimal to balance spatial resolution and penetration depth [75]. We chose a wavelength of 650nm because it had higher quantum efficiency for the process. For a numerical aperture of 1 and magnification of 0.5, the speckle size is approximately 2.3µm, which corresponds to a pixel size of 5µm x 5µm. This can be adjusted by changing the magnification or numerical aperture.

Section 3.2.1: Shot noise considerations:

The image sensor is expected to be used in a hand held optical device. The light from the laser must be a safe level to avoid damage to the eye. A light level of 10µW/cm² was chosen, and this level was well below the safe level specified by international standards [76] [77]. Thus it provides a little room to increase the irradiance of the laser to raise the signal to noise ratio.
In order to estimate the amount of light at the image sensor plane, the loss of intensity at each stage of the hand held optical setup was estimated. The laser first reflects off of the eye, goes through a beam splitter and an aperture before hitting the pixel. About 5-10% of the incident light is reflected off of the retina [78], 50% of that passes through the beam splitter, and 45% of that hits the image sensor. Thus approximately 1% of the light that hits the eye arrives at the image sensor. If 10µW/cm² hits the eye, then approximately 100nW/cm² will hit the image sensor assuming a magnification of one.

The number of photons that will hit the image sensor also depends on the exposure time. Increasing the exposure time will increase the number of photons hitting the image sensor and therefore the Signal to Noise ratio (SNR). However, microsaccades occur around a rate of 1 Hz [79]. For time based LSCI used previously be Rege et. al, a stack of 80 images need to be captured in approximately one second [80]. This corresponds to an exposure time of about 12.5 milliseconds. In order to achieve more light, this was relaxed to 16.667 milliseconds, or 60 frames per second. In order to maximize exposure time, the pixel was designed for rolling shutter. The quality of Laser Speckle Images is also sensitive to exposure time [80], so programmable exposure time was implemented. See Section 3.4: Pixel Operation for details.

A fill factor of 40% was chosen as a target based on previous designs using the capacitive trans-impedance Amplifier (CTIA) pixel design. In previous work, the fill factor for a CTIA pixel design has been at most about 40% [49] [81] [82] [83] [84]. For comparable processes, a fill factor of 26% was achieved in a 0.35µm process by Zhang et al. for a 9.5µm x 9.5µm pixel [9]. In the 0.5µm process, Murari et al. achieved a fill factor of 41% with a 20.1µm x 20.1µm pixel, and in the 0.25µm process, a fill factor of 40% was achieved by Furuta et al. [83]. By using a sharing structure, the fill factor for this pixel design would be increased.

The pixel size was 10µm x 10µm for several reasons. Firstly, in order to achieve a fill factor of 40%, the pixel size should be similar to the pixel in Zhang et al. because a similar process was used. Secondly, in order to capture a wide field of view with sufficient resolution, a fairly large array size is needed. A 30µm feature on the retina will be imaged as 20µm by using a magnification of 0.67 for an 800 x 800 array of pixels to achieve a field of view of 12mm x 12mm on the retina. A 10µm pixel was the best size as a trade-off between resolution, field of view and shot noise. Finally, a 10µm pixel pitch gives more room to for the column parallel analog to digital converters that will require more wiring.
Assuming our imager is shot noise limited and has a quantum efficiency of 67%, we can calculate the expected signal to noise ratio. The number of photons hitting a pixel can be found based on the pixel size, wavelength, irradiance and exposure time. The energy of a photon at a specific wavelength is given by Planck’s equation:

\[ E_{\text{photon}} = h \nu = \frac{hc}{\lambda} = \frac{6.626 \times 10^{-34} (J \cdot s) \times 2.998 \times 10^8 (m/s)}{6.50 \times 10^{-9} m} = 3.056 \times 10^{-19} J \]  

(3.2)

where \( h \) is Planck’s constant, \( c \) is the speed of light and \( \lambda \) is the wavelength of light.

The total energy irradiated onto a pixel during one exposure cycle is given by:

\[ E_{\text{pixel}} = \text{Irradiance} \times \text{exposure time} \times \text{pixel area} \]  

(3.3)

\[ E_{\text{pixel}} = \left( \frac{100 \times 10^{-9} W}{10^{-4} m^2} \right) \times (16.667 \times 10^{-3} s) \times (10 \times 10^{-6} m)^2 = 1.667 \times 10^{-15} J \]

Thus, the number of photons (NP) is given by:

\[ NP = \frac{E_{\text{pixel}}}{E_{\text{photon}}} = 5.454 \times 10^3 \text{ photons} \]  

(3.4)

Since Quantum Efficiency (QE) is defined as the number of electrons per incident photon, then the number of electrons (NE) is the number of photons hitting the photodiode multiplied by the quantum efficiency:

\[ NE = NP \times QE \times \text{Fill Factor} \]  

(3.5)

\[ NE = (5.454 \times 10^3 \text{photons}) \times (0.67) \times (0.40) = 1.462 \times 10^3 \text{electrons} \]

Light shot noise power is modeled as

\[ \sigma_e^2 = \mu_e = NE \]  

(3.6)

Thus the signal to noise ratio is given by:

\[ SNR = 20 \times \log_{10} \left( \frac{NE}{\sigma_e} \right) = 20 \times \log_{10} \left( \frac{NE}{\sqrt{NE}} \right) = 20 \times \log_{10} \left( \sqrt{NE} \right) = 31.65 dB \]  

(3.7)

Stacks of 80 images taken from a CCD 12-bit camera were artificially degraded to different bit levels, and the percent error between the 12-bit LSCI images and the degraded LSCI images were calculated. This was done for eight different images, and the worst case was selected for table 1 below. Image stacks were taken of rat brains courtesy of Abhishek Rege.
Table 3.1: Simulated Laser Speckle Image degradation

<table>
<thead>
<tr>
<th>Number of bits</th>
<th>SNR (dB)</th>
<th>Worst image mean error over blood vessels</th>
<th>Worst image mean error</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>24</td>
<td>82.61%</td>
<td>49.93%</td>
</tr>
<tr>
<td>5</td>
<td>30</td>
<td>28.45%</td>
<td>16.19%</td>
</tr>
<tr>
<td>6</td>
<td>36</td>
<td>8.34%</td>
<td>4.92%</td>
</tr>
<tr>
<td>7</td>
<td>42</td>
<td>2.55%</td>
<td>1.64%</td>
</tr>
<tr>
<td>8</td>
<td>48</td>
<td>0.99%</td>
<td>0.68%</td>
</tr>
<tr>
<td>9</td>
<td>54</td>
<td>0.48%</td>
<td>0.35%</td>
</tr>
</tbody>
</table>

![Image 7 RTD1: 12 bit LSO1 Image Using 80 Raw Images](image1)

![Image 7 RTD1: 5 bit LSO1 Image Using 80 Raw Images](image2)

![Image 7 RTD1: Error between 12-bit and 5-bit](image3)

![Image 7 RTD1: Error between 12-bit and 5-bit for vessel pixels](image4)

Mean error = 16.192%  Median error = 9.6551%  Max error = 20.1166%  Mean error = 28.4553%  Median error = 17.3971%  Max error = 30.6478%

Figure 3.1: Image corresponding to largest error after converting a 12-bit image stack to a 5-bit image stack. This corresponds to the degradation expected for the estimated SNR.
Due to fabrication limitations with the foundry for the particular type of run we were doing, the chip size was later limited to 8mm by 9mm. For a first prototype, the pixel array size was reduced to 480 by 480 pixels to fit the chip size limitation. With the change in array size, the frame rate was changed to 100 frames per second. Because programmable exposure time was implemented, the chip could still be run with an exposure time of 16.667msec, so the calculations above are still valid.

Section 3.3: Pixel Circuit Design:

A capacitive trans-impedance amplifier pixel design (CTIA) was used. A mathematical description of how a CTIA pixel operates can be found in Section: 2.2.4.5: Capacitive Transimpedance Amplifier APS (CTIA APS). Due to the minimum poly-poly capacitor size of the process, a sharing structure was used in the CTIA. Sharing occurred in multiple places in the circuit to increase fill factor. First a single amplifier was shared across four pixels to reduce the number of transistors in a pixel. A cascaded common source amplifier was used as the in-pixel amplifier for the CTIA structure. Secondly, the PMOS transistors of the amplifier were shared for a column. This has several advantages at the cost of speed: no PMOS transistors in the pixel gives more space for the photodiode because of NWELL spacing rules, and only the amplifier that is being read out draws current. Finally, some of the feedback capacitors used by the amplifier are shared by two adjacent amplifiers. This was done to maintain a high fill factor while decreasing the feedback capacitance by putting multiple capacitors in series to increase sensitivity. Diodes were added to the floating nodes between the series capacitors to ensure the voltage does not get too high and cause device breakdown. Bias voltages vcasn, pixel_bias, and pixel_casp were generated on chip using a 9µA bias current. A 9µA current was necessary for the output of the amplifier to settle within 20.825µs, which corresponds to a frame rate of 100 FPS in the rolling shutter scheme. The NMOS transistors in the cascoded common source amplifier (M1, M2) were sized to maximize DC gain at about 860 for this current draw (see Figure 3.2). The lengths were chosen to be twice the minimum size to decrease fabrication variability. M3 is a switch that connects the NMOS part of the amplifier to the column line to the shared PMOS current source and activates the amplifier. It was sized to allow enough current to flow through for the amplifier while minimizing charge injection and clock feed through. The switches that connect the
photodiode nodes to the input of the amplifier (M4, M5, M6, M7) were minimum sized to minimize charge injection and clock feed through. A transistor level schematic of a group of 8 pixels is shown in Figure 3.2.

Figure 3.2: A: Transistor level schematic of a group of 8 pixels in a single column. The value of the capacitors, C, was 10.7fF, the smallest capacitance for this process. Diodes were implemented as n+/psub to minimize area. B shows the bias circuit for generating the pixel biases [85]. The generation of pbias and vcasn will be discussed in Section: 4.3.8.2. C: Layout implementation of a group of 8 pixels.
Section 3.4: Pixel Operation

The pixel exposure time can be programmed. This was implemented for exposure times less than 10msec by resetting the pixel again to shorten its exposure time with a resolution of 20.825µs. This method has a minimum exposure time of 20.825µs. For exposure times above 10msec, an externally controlled enable pin could pause or run the digital clock signals. A timing diagram for an exposure time of 10msec is shown below in Figure 3.3 and a timing diagram for an exposure time of 20.825µs is shown in Figure 3.4.

The signal Rs<x> is the row select pixel for row x and corresponds to RSX in Figure 3.2. Rst_shared<x> or RST_SX in Figure 3.2 is the reset signal for a group of four pixels and resets rows x to x+3. Rs_shared<x> or RS_SX in Figure 3.2 is a shared row select signal that selects an amplifier for a group of four pixels and connects it to the column line. The amplifier selected corresponds to pixels in rows x to x+3.

For 10msec exposure time operation, the overall timing diagram is shown for the first 8 pixels in Figure 3.3A. Rs_shared<x> signal is first brought high to select the amplifier for a group of four pixels. Simultaneously, the Rst_shared<x> signal is also brought high to reset the node at the input of the amplifier (gate of M1) before a row is selected. This is to ensure that the charge at the gate of M1 is the same for different rows before the charge from the photodiode is deposited at the gate of M1. Once Rst_shared<x> is released, a row select (Rs<4x>) signal is raised to select a row. This dumps the charge from the photodiode to the input of the gate, and the amplifier makes the output voltage equal to the amount of charge from the photodiode divided by the feedback capacitance. Once the data is grabbed by the Analog to Digital converter, the photodiode voltage that was just read out is reset (Rst_shared<x>). After the pixel is reset, the Rs<4x> signal is lowered; the Rst_shared<x> signal stays high to keep the gate of M1 at the reset voltage. The next Rs signal (Rs<4x+1>) is not raised because there is an allotted time here for a delayed reset for shorter exposure times (Figure 3.3B). This procedure is repeated for the next three pixels shared by an amplifier. After finishing the readout of the last pixel of an amplifier group, the reset signals for that amplifier (Rst_shared<x>) and the next amplifier (Rst_shared<x+1>) are raised at the same time so that the gate of M1 of the next amplifier is driven to a voltage near the reset level of the next amplifier (Figure 3.3C). Rst_shared<x> is then lowered when Rs_shared<x> is lowered, signaling the end of that amplifier’s operation. This way, when the next amplifier is activated with the rising edge of Rs_shared<x+1>, the...
voltage at the gate of M1 of the next group quickly settles to the reset voltage. The same readout pattern is then repeated for this group of four pixels and for the rest of the column.

For exposure times less than 10msec, operation is very similar. The only difference is a delayed reset signal that happens after the falling edge of row select (Rs<4x>). In order to reset a pixel, the pixel must be selected (Rs<4x>), the amplifier must be selected (Rs_shared<x>), and the reset switch for that amplifier must be turned on (Rst_shared<x>). During the time Rs is low and the next Rs is not high yet, the signals for the delayed reset (Rs<4x>, Rs_shared<x>, Rst_shared<x>) are brought high to reset a previous pixel again to achieve a shorter exposure time. Before the next Rs is brought high, the delayed reset signals are brought low, and the reset signal for the next pixel is brought high to set the voltage at the gate of M1 to the reset level. This can be seen more clearly in **Figure 3.4B**. A 9 bit number controlled from off chip controls the exposure time by specifying the number of delays before an additional reset happens for a pixel. A code of all ones for the 9 bit control signal turns off the enable signal. This pauses all digital clocks in the pixel and ADC to achieve exposure times higher than 10msec.
Figure 3.3: Timing diagram of a group of 8 pixels within a column operating at an exposure time of 10msec. A shows the overall timing diagram, B shows the timing of the reset signal in relation to the row select signals of the same amplifier, and C shows the timing of the reset signals in relation to row select signals from different amplifiers.
Figure 3.4: Timing diagram of a group of 8 pixels within a column operating at an exposure time of 20.825µs. A shows the overall timing diagram, B shows the timing of the reset signal in relation to the row select signals of the same amplifier, and C shows the timing of the reset signals in relation to row select signals from different amplifiers.
Section 3.5: Pixel Simulation results:

The pixel was simulated in several ways to characterize its performance. Shown in Figure 3.5 is a nominal AC simulation looking at gain by sweeping frequencies between 0.1Hz to 1GHz. The amplifier has a bandwidth of 1.19MHz and a DC gain of about 860. Higher gain would mean there is less distortion from the amplifier stage with the distortion being about $\frac{1}{\text{gain}}$.

![Gain of Pixel Amplifier](image)

**Figure 3.5:** Simulation results for the gain of the pixel amplifier at different frequencies. The bandwidth is about 1.19MHz.

For transient simulations, the photodiode was modeled as a current source in parallel to a capacitor (see Figure 3.6). The current going through the current source represents the light hitting the photodiode. In order to estimate the value for the current source, the fill factor of the pixel was estimated based on a few factors. Different fill factors can be based on areas covered by certain layers. Since there are essentially two photodiodes per pixel (p+/nwell/psubstrate has a diode from the p-substrate to the nwell, and from the p+ active
to the nwell), the quantum efficiency of the area covered by both diodes should be higher than the quantum efficiency only covered by one of the diodes. Furthermore, the area not covered by the silicide block layer should have a lower quantum efficiency compared to the area covered by the silicide block layer [86]. Finally, the area covered by metal should block most of the light. For these estimations, we will use the drawn area as the estimated area.

We can consider three different ways to estimate the fill factor of the pixel, and the actual fill factor would be somewhere between the three values. One way to estimate the fill factor is to use the area given by the overlap of the photodiode and silicide block layer. With this estimate, the fill factor is 21.4%. A very optimistic estimate of fill factor is to include the full photodiode area that is not covered by metal; with this estimate, the fill factor is 39.0%. Finally, the most accurate way to estimate fill factor is to have different quantum efficiencies for each group of layers. For example, the layer with both photodiode types and silicide block layer would have the highest quantum efficiency, and the estimated quantum efficiencies for both photodiodes are used for that area. Next, the area with only the nwell/psub type photodiode would have a quantum efficiency corresponding to that sort of photodiode. Finally, the photodiode area not covered by silicide block would have even lower quantum efficiency. Since the actual quantum efficiency is not known until fabrication, the quantum efficiencies of the various cases were adjusted relative to the quantum efficiency of both photodiodes together so that the expected resolution could be plotted against the quantum efficiency (see Figure 3.7). Calculations of signal to noise ratio were only based on shot noise, and were done using equations (3.2) - (3.7) with appropriate fill factor and quantum efficiency values. Next, the expected number of electrons is calculated from equations (3.2)-(3.5) using the different fill factors and quantum efficiencies. The current source in Figure 3.6 can be estimated by using the following equation:

$$\text{Average Current} = \frac{NE \times 1.602 \times 10^{-19}}{\text{exposure time}} \left(\frac{\text{Coulombs}}{\text{electron}}\right)$$

(3.8)
Figure 3.6: Model of photodiode used in simulation. A value of 19.7fF was used for the capacitor in the model based off of extracted parameters from the layout. A value of 10fA was used for the current source for expected light levels of 100nW/cm².

Using the different estimations of fill factor, we get 7.52fA for the lowest fill factor estimate, 13.70fA for the highest fill factor estimate, and 9.13fA for the weighted fill factor estimate. Given this range, we chose use 10fA in the simulations as the current source corresponding to the expected light level.
Figure 3.7: Maximum theoretical Signal to Noise ratio as a function of quantum efficiency based on light level of 100nW/cm$^2$ at 650nm with an exposure time of 16.667msec based on different estimations of fill factor. For this process, we estimated a quantum efficiency of about 67%, which is indicated by the dashed blue line. For the best estimate using different weighted quantum efficiencies, the expected SNR using the estimated quantum efficiency is 29.77dB.

In order to characterize the dynamic range and matching characteristics of the pixel, transient simulations were done on a group of 8 pixels. For better accuracy, groups of 8 dummy pixels were placed all around the group of 8 pixels, so that the total array simulated was 3 rows by 24 columns. The layout of the array was then extracted for parasitic resistances and capacitances for simulation. The same photodiode model was used across all pixels with the same current. The current level was swept across the full range of the pixel in discrete steps (see Figure 3.8 for current levels used). The group of 8 pixels were sequentially read out as they would be in normal operation, so each level going horizontally (across time) in Figure 3.8 represents a different pixel, and each level going vertically represents a different current level sweep.
Figure 3.8: Transient Simulations with different current levels for a group of eight pixels. This was used to derive matching and dynamic range characteristics in Figure 3.9 and Figure 3.10.

To measure linear dynamic range of the pixel output, the voltage output of the last pixel (the right most signal in Figure 3.8) was plotted against the photodiode current level. A line was fitted to it, and the range where the points stayed within 0.1V of the line was taken to be the linear dynamic range.
Figure 3.9: Linear dynamic range of the pixel is 2.097V. The slope of the fit line is used to calculate the feedback capacitance value.

For characterizing the level of mismatch between pixels in a group of 8, the voltage outputs of the different pixels were compared at the expected light level, which corresponds to the 10fA current source (Figure 3.10). Because the layouts were not perfectly symmetric, the parasitic capacitances between the row select lines and the photodiodes did not match. In the layout, every effort was made to match these parasitic capacitances as closely as possible.
Figure 3.10: Transient simulation showing the matching characteristics between the 8 pixels of a layout group at the expected light level (current source set to 10fA). The largest difference in output values was 98.32mV.
Figure 3.11: Input referred noise simulation of pixel amplifier. The RMS noise integrated from 1Hz to 1MHz is 101.065µV.

Next to get an idea of the noise after the amplifier stage, the noise of amplifier was simulated across different frequencies at integrated (see Figure 3.11). However, in order to compare the noise from the amplifier and shot noise, the noise at the photodiode itself must be considered, not at the input of the amplifier. Since during normal operation, the light signal is just accumulating on the capacitance of the photodiode itself and is disconnected from the amplifier, the capacitance of the photodiode will be considered as the input node; the noise from the amplifier and shot noise will be compared at the input node. The voltage at the input node of the amplifier is the integrated photodiode current divided by the capacitance at that node. The capacitance at the input of the amplifier includes the capacitance of the photodiode and the feedback capacitance.
The voltage at the photodiode is given by

\[ V_{pd} = \int \frac{I_{pd}}{C_{pd}} \]  

(3.10)

This can also be rewritten as

\[ V_{pd} = \left( \frac{C_{pd} + C_{fb}}{C_{pd}} \right) V_{input \text{ amplifier}} \]  

(3.11)

The extraction of the photodiode capacitance parameter was from the layout capacitance extraction tool and the feedback capacitance parameter is from Figure 3.9. To calculate the total noise from the pixel and shot noise, the noise powers are added, and to calculate the signal to noise ratio, the signal voltage at the photodiode is divided by the square root of the sum of the noise powers.

First convert number of electrons (NE) of the signal \((V_s)\) to a voltage level at the photodiode

\[ V_s = \frac{\text{NE} \times 1.602 \times 10^{-19} \text{ Coulombs}}{\text{electron}} \]  

(3.12)

The shot noise \((N_s)\) value is given the square root of the signal value, and the amplifier noise \((N_a)\) is given by equation (3.11) after plugging in the input referred amplifier noise for \(V_{input \text{ amplifier}}\).

The total RMS input referred noise \((N_{IRN})\) is then

\[ N_{IRN} = \sqrt{N_s^2 + N_a^2} \]  

(3.13)

The RMS noise level at the output \((N_{pixel})\) is given by the RMS input noise multiplied by the gain from the photodiode to the output of the pixel amplifier.

\[ N_{pixel} = \left( \frac{C_{pd} + C_{fb}}{C_{pd}} \right) \left( \frac{C_{pd}}{C_{fb}} \right) (N_{IRN}) = \frac{C_{pd} + C_{fb}}{C_{fb}} (N_{IRN}) \]  

(3.14)

The expected signal to noise ratio at the output of the pixel is
\[ SNR_{\text{pixel}} = 20 \log_{10} \left( \frac{V_s}{\sqrt{N_s^2 + N_R^2}} \right) \]  \hspace{1cm} (3.15)

The results of these expected noise and resolution calculations are shown in Table 3.2.

Table 3.2: Expected Noise Levels and SNR after Pixel

<table>
<thead>
<tr>
<th></th>
<th>Silicide Block Area Fill Factor Estimate</th>
<th>Weighted QE estimation of fill factor</th>
<th>Max Fill Factor Estimate</th>
</tr>
</thead>
<tbody>
<tr>
<td>NE</td>
<td>782 electrons</td>
<td>950 electrons</td>
<td>1425</td>
</tr>
<tr>
<td>( V_s )</td>
<td>6.4mV</td>
<td>7.7mV</td>
<td>11.6mV</td>
</tr>
<tr>
<td>( N_s )</td>
<td>227.1909µV</td>
<td>250.64µV</td>
<td>306.98µV</td>
</tr>
<tr>
<td>( N_{IRN} )</td>
<td>253.4µV</td>
<td>274.63µV</td>
<td>326.86µV</td>
</tr>
<tr>
<td>( N_{\text{pixel}} )</td>
<td>2.3mV</td>
<td>2.5mV</td>
<td>3mV</td>
</tr>
<tr>
<td>Signal to Noise Ratio</td>
<td>27.984dB</td>
<td>28.955dB</td>
<td>31.001dB</td>
</tr>
</tbody>
</table>
Chapter 4: Column Parallel 2.8074 Bit per Cycle Cyclic Analog-to-Digital Converter

Section 4.1: Selection of Architecture

For this chip, the original array size was 800 by 800 pixels, the frame rate was 60 frames per second, and the desired ADC resolution was 10 bits. For the approximately 2V linear dynamic range, this means one LSB is about 1.95mV. Since the pixel noise ranges from 2mV to 3mV depending on the actual fill factor, the noise level of the pixel is approximately one LSB in the ADC, which is ideal. For this imager, the signal to noise ratio will not exceed 48dB (or 8 bits). However, in order to minimize the quantization noise injected into the system from the ADC, we decided to design a 10 bit ADC. At a frame rate of 60 frames per second, the ADC will need to convert 800 signal values in 16.67ms, resulting in 20.83 µs per conversion. After the design was modified for a 480 by 480 pixel array, the ADC sampling rate was kept the same. A single-slope ramp will require the comparator settle within 20.36 ns, and a MRSS will require the comparator settle within m*20.36 ns. For 10 bits, the second order Sigma-Delta architecture requires 45 clock cycles which gives about 463 ns per clock. For Cyclic and SAR architectures, the comparator needs to settle within 2.083 µs.

For these relatively low speeds, pipeline ADC architecture is not needed and a SAR ADC with its lower power and area would be preferred over a pipelined architecture. Using a single-slope ramp would require designing a powerful ramp driver and fast comparator. A MRSS has the same problem, and in order to relax the ramp driver specifications, many ramps would be needed which requires many comparators. A charge redistribution SAR ADC requires a very large area for capacitors for the selected process and is thus not a viable option. 10-bit resolution SAR ADCs often requires gain correction circuitry [66]. This can be relaxed by using a hybrid structure as discussed above so that multiple bits are digitized per step, which reduces the number of stages and thus the constraint on gain. The circuits required for a multiple bit digitization per step will be similar with an amplifier for the sample / hold stage, an amplifier for the MDAC stage, and a comparator. A first and second order delta sigma architectures have similar complexity to a multi-bit per stage cyclic ADC. Thus given the constraints of the design, a multi-bit per stage cyclic
ADC or a delta sigma ADC would be best. For this design, a multi-bit per stage cyclic ADC was implemented.

**Section 4.2: Algorithm**

The output from the pixel first goes through a Double Delta Sampling (DDS) circuit to help cancel off some of the reset noise. The DDS circuit also adds a voltage offset to put the output voltage into the correct input range of the ADC. The ADC then digitizes the voltage in five steps, where each step digitizes the voltage to 2.8074 bits. Similar to the 1.5 bit per stage algorithms implemented in cyclic and pipelined ADCs, the extra partial bits help handle the effects of comparator offset so that the comparator offset manifests as a constant offset of the digitized output instead of distorting the algorithm. After each stage, the MDAC calculates the residue and amplifies by a gain of 4 and feeds that into the next step. The 2.8074 bit result from each step (recorded as 3 bits) are weighted and added together to form the final 10 bit output. The details of each step will be broken down mathematically for a general multi-bit per cycle ADC and described below.

For notation purposes, let us first define the following variables. The output of the sample hold stage will be written as \( x_n \) where \( n \) is the step or cycle number. The output of the MDAC stage will be written as \( y_n \), the quantization noise will be written as \( e_n \), the inter-stage gain will be written as \( y \), the digitized signal will be written as \( d_n \), the fed back Digital-to-Analog (DAC) voltage will be written as \( q_n \) for step \( n \), and \( b_n \) is the comparator offset for step \( n \).

First the output of the DDS is sampled by the sample / hold circuit.

\[ x_0 = V_{DDS} \quad (4.1) \]

The first stage then digitizes it to the desired number of bits per cycle with a DAC value close to the actual value with some quantization error and comparator offset.

\[ q_1 = x_0 + e_1 - b_1 \quad (4.2) \]

The MDAC calculates the residue by subtracting the digitized signal from the sample / hold signal and amplifies it by the inter-stage gain. In real circuit implementation, it will do this around some voltage \( V_{ref} \).
\[ y_1 = \gamma(x_0 - q_1) + V_{ref} = \gamma(x_0 - (x_0 + e_1 - b_1)) + V_{ref} = \gamma(b_1 - e_1) + V_{ref} \quad (4.3) \]

The second cycle is started by sampling the output of the MDAC stage:

\[ x_1 = y_1 \quad (4.4) \]

Equations (4.2) to (4.4) can be generalized to the different stages:

\[ q_n = x_{n-1} + e_n - b_n \quad (4.5) \]

\[ y_n = \gamma(x_{n-1} - q_n) + V_{ref} = \gamma(x_{n-1} - (x_{n-1} + e_n - b_n)) + V_{ref} = \gamma(b_n - e_n) + V_{ref} \quad (4.6) \]

\[ x_n = y_n \quad (4.7) \]

Now the equations for each digitized output will be written so that we can combine them to reconstruct the original signal:

\[ q_1 = V_{DDS} + e_1 - b_1 \quad (4.8) \]

\[ q_2 = x_1 + e_2 - b_2 = (y_1) + e_2 - b_2 = \gamma b_1 - \gamma e_1 + e_2 - b_2 + V_{ref} \quad (4.9) \]

\[ q_3 = x_2 + e_3 - b_3 = (y_2) + e_3 - b_3 = \gamma b_2 - \gamma e_2 + e_3 - b_3 + V_{ref} \quad (4.10) \]

\[ q_4 = x_3 + e_4 - b_4 = (y_3) + e_4 - b_4 = \gamma b_3 - \gamma e_3 + e_4 - b_4 + V_{ref} \quad (4.11) \]

\[ q_5 = x_4 + e_5 - b_5 = (y_4) + e_5 - b_5 = \gamma b_4 - \gamma e_4 + e_5 - b_5 + V_{ref} \quad (4.12) \]

Or in general:

\[ q_n = \gamma b_{n-1} - \gamma e_{n-1} + e_n - b_n + V_{ref} \quad (4.13) \]

Now we weight the digitized result of each cycle to cancel some \( e_n \) terms when they are summed:

\[ \gamma^4 q_1 = \gamma^4 V_{DDS} + \gamma^4 e_1 - \gamma^4 b_1 + \gamma^4 V_{ref} \quad (4.14) \]

\[ \gamma^3 q_2 = \gamma^4 b_1 - \gamma^4 e_1 + \gamma^3 e_2 - \gamma^3 b_2 + \gamma^3 V_{ref} \quad (4.15) \]
\[ y^2 q_3 = y^3 b_2 - y^3 e_2 + y^2 e_3 - y^2 b_3 + y^2 V_{ref} \]  
\[ y q_4 = y^2 b_3 - y^2 e_3 + ye_4 - yb_4 + yV_{ref} \]  
\[ q_5 = y b_4 - ye_4 + e_5 - b_5 + V_{ref} \]

Now the weighted values are summed together and \( V_{ref} \) is put on the other side:

\[ \sum_{i=1}^{5} y^{5-i} (q_i - V_{ref}) = y^4 V_{DDS} + e_5 - b_5 \]  
\[ \sum_{i=1}^{n} y^{n-i} (q_i - V_{ref}) = y^{n-1} V_{DDS} + e_n - b_n \]

Now if the DAC output values can be written in terms of the digital values by scaling and adding the voltage reference offset:

\[ q_n = \rho d_n + V_{ref} \]  
\[ \rho \] is the scaling factor between the digital signal and the DAC.

Substituting equation (4.21) into (4.20) yields

\[ \sum_{i=1}^{n} y^{n-i} (\rho d_i) = y^{n-1} V_{DDS} + e_n - b_n \]

From this equation, it’s clear how an imprecise inter-stage gain can distort the digital output because it is raised to the n-1 power. If a normal 1.5 bit per cycle algorithm is used, \( n \) would be 10 for this design and \( y \) would be 2. By digitizing at least 2.5 bits per stage, \( n \) would only be 5, which greatly reduces the need for precise gain; on the left side of the equation, the weighted values are done digitally while on the right side of the equation, the multiplication by \( y^{n-1} \) is done in the analog domain. If they are not matched, then the equation no longer holds. This is how the error from imperfect gain accumulates with the number of stages.
There are several constraints that the equations reveal. In order to correctly digitize the input voltage, \( e_n \) should decrease every cycle so that final error value is very small (less than 1 LSB). In order to do this, the DAC estimate of the voltage from the sample / hold stage must be less than the difference between adjacent DAC voltage reference values. Therefore, the DAC voltage reference values should extend to at least the range of the input voltage from the DDS stage.

The inter-stage gain should be a multiple of 2 for easy implementation of multiplication in the digital domain. The product of the inter-stage gain and difference between adjacent DAC voltage references (or the maximum difference the MDAC needs to amplify) should be equal to the full input range of the ADC. Since the full input range of the ADC is 2V, if the inter-stage gain is 2, then the difference between DAC voltage levels needs to be 1V. For an inter-stage gain of 4, the difference between DAC voltage levels is 0.5V, and for a gain of 8, the difference between DAC voltage levels is 0.25V. Since the supply voltage for this process is 3.3V, and an algorithm of at least 2.5 bits per cycle requires a minimum of 5 levels, implementing a gain of 2 would not work. A gain of 4 works well since 5 levels of 0.5V covers the range perfectly. For a gain of 8, at least 9 different levels are needed, which makes it a 3.5 bit per cycle algorithm. Furthermore, achieving a precise gain of 8 is more difficult because it either requires a many clock cycles if the gain is made immune to capacitor mismatch or large capacitors if it relies on capacitor ratios. Thus a gain of 4 and a difference of 0.5V for adjacent DAC voltage references were selected. Comparator references are placed halfway between each DAC voltage reference so that the DAC reference represents the best estimate of the voltage signal.

The digital values \( d_n \) can take the following values: \(-3,-2,-1,0,1,2,3\). For a true 2.5 bit per cycle design, only 5 levels are needed \((-2,-1,0,1,2\); however, in order to handle non-ideal devices, the extra levels are needed. To see why, consider the case when the input voltage value is 1.8V.

\[
x_0 = 1.8V
\]  

(4.23)

If we use a 2.5 bit per cycle algorithm, the comparator references will fall at 0.9V, 1.4V, 1.9V, 2.4V assuming the DAC voltage references are centered about \( V_{ref} = 1.65V \), the midpoint of the supply voltage. The digitization occurs as follows: the comparator starts at the lowest reference voltage and switches to higher comparator voltages until the output of the comparator changes. Once it changes, the digital value is
stored and a DAC reference voltage is selected to be halfway between the selected comparator reference voltage and the comparator reference voltage below it.

For the example, the first comparator value that exceeds the input voltage 1.8V is 1.9V; however, if there is a comparator offset exceeding 100mV such that the comparator output changes at the 2.4V reference instead, then the selected DAC voltage is

\[ q_1 = 2.15V \]  

The MDAC output is then given by

\[ y_1 = 4(1.8V - 2.15V) + 1.65V = 0.25V \]  

Then the signal is sampled

\[ x_1 = 0.25V \]  

The comparator will then select the lowest possible reference:

\[ q_2 = 0.65V \]  

\[ y_2 = 4(0.25V - 0.65V) + 1.65 = 0.05V \]  

\[ x_2 = 0.05V \]  

\[ q_2 = 0.65V \]  

\[ y_3 = 4(0.05V - 0.65V) + 1.65 = -0.75V \]

A negative voltage occurs, and the actual voltage in the circuit will again be 0V. This repeats until the ADC is done digitizing. The resulting digital bits from each bit are: 1,-2,-2,-2,-2; the digital output is then 86 (from a range of -512 to 511). Ideally the digital bit outputs should be: 0, 1, 1,-1, 1 which results in a digital output of 85. Although the algorithm can handle it to a degree; however it will give the same result for any voltage below 1.8375V. Thus the algorithm has saturated for a large enough comparator offset.

In order to handle this, additional DAC levels were added so that there are 7 levels in all, resulting in 2.8074 bits per cycle. Now the new comparator levels are 0.4V, 0.9V, 1.4V, 1.9V, 2.4V, 2.9V, and the
new DAC voltage references are 0.15V, 0.65V, 1.15V, 1.65V, 2.15V, 2.65V, 3.15V. If we repeat the previous example using 2.8074 bits per cycle and assume constant comparator offset of 110mV, we get

\[ x_0 = 1.8V \] (4.32)

\[ q_1 = 2.15V \] (4.33)

\[ y_1 = 4(1.8V - 2.15V) + 1.65V = 0.25V \] (4.34)

\[ x_1 = 0.25V \] (4.35)

\[ q_2 = 0.15V \] (4.36)

\[ y_2 = 4(0.25V - 0.15V) + 1.65 = 2.05V \] (4.37)

\[ x_2 = 2.05V \] (4.38)

\[ q_3 = 2.15V \] (4.39)

\[ y_3 = 4(2.05V - 2.15V) + 1.65 = 1.25V \] (4.40)

\[ x_3 = 1.25V \] (4.41)

\[ q_4 = 1.65V \] (4.42)

\[ y_4 = 4(1.25V - 1.65V) + 1.65 = 0.05V \] (4.43)

\[ q_5 = 0.65V \] (4.44)

The ADC is able to recover from saturation, and the output digital bits are: 1, -3, 1, 0, -2, yielding a result of 78. If the input voltage is changed to 1.82V with the same offset, the output digital bits become: 1, -2, -2, -2, -1. The resulting value is 87, which is relatively correct compared to the 1.8V value. A difference of 20mV at the input should manifest as approximately 10 LSBs, which the 2.8074 bit per cycle reflects; thus having 7 levels to digitize to per stage allows the algorithm to handle larger comparator offset.
Section 4.3: Circuit Implementation of ADC

A block diagram of the circuit implementation is shown in Figure 4.1. The pixel first enters the DDS stage where a pixel reset voltage is subtracted off the signal and a DC offset is added. The output of the DDS passes through the MUX and is sampled and held by the Sample / Hold stage. Simultaneously, the comparator compares the DDS output to the comparator voltage references. The comparator voltage reference starts at the lowest voltage, 0.4V, and cycles through the voltages until the output of the comparator changes. The references then stops switching and DAC voltage reference for the MDAC is selected using the digital logic block. Here the digital logic block also saves the digitized value (-3 to 3). The MDAC subtracts off the appropriate DAC voltage reference from the output of the Sample / Hold stage and multiplies it by the inter-stage gain of 4. The output of the MDAC is fed to the MUX which goes to the Sample / Hold stage for the next cycle. After 5 cycles, the digital bits are weighted accordingly, and the

Figure 4.1: Block Diagram of Circuit implementation of 2.8074 bit per cycle ADC. The multiplexer (MUX) was implemented using two of the switches shown in Figure 4.3.
output is shifted off chip. The output is 11-bits with the extra bit to handle saturation so that the sign bit will never flip from saturation.

**Section 4.3.1: Double Delta Sampling Circuit**

For a 10-bit system, we would like to map the full range from the DDS circuit to the full range of the ADC. To maximize the dynamic range of the ADC, the DDS output should be mapped to the center of the range of the ADC. Thus, the DDS needs to be able to both cancel part of the reset noise and add a constant DC offset in order to put it into the correct input range of the ADC. A simple version of a DDS

**Figure 4.2:** DDS Circuit Implementation. A shows the overall circuit implementation. B shows the design of the amplifier. C shows the circuit during the sampling phase, and D shows the circuit during the hold phase. E shows the timing of the clocks that control the DDS circuit. F shows the layout of the DDS stage. Capacitors were implemented using Double Metal-Insulator-Metal (DMIM) capacitors.
circuit that cancels part of the reset noise was taken and modified from Zhang et al. [81]. By switching the ground node to a voltage bias, the voltage at the output of the DDS has an offset equal to the voltage bias. Figure 4.2 shows the overall circuit and operation. Figure 4.3 shows the implementation of switches in the DDS and other blocks in the ADC. Unlike the sample / hold and MDAC stages in the ADC, the closed loop gain of the DDS circuit does not need to extremely high. Thus a cascoded common source amplifier was chosen for its simplicity and low transistor count, which results in less area and power.

During the sample operation (see Figure 4.2), the input of the amplifier gets driven to the inversion point of the amplifier, which we will call $V_{\text{ref}}$. Thus we can write the equations for the charge across $C1$ and $C2$.

$$Q_{\text{sample}}^1 = C1(V_{\text{ref}} - V_{\text{sig}}) \quad (4.45)$$

$$Q_{\text{sample}}^2 = C2(V_{\text{ref}} - V_{\text{con}}) \quad (4.46)$$
Q1 is the charge across capacitor C1, and Q2 is the charge across capacitor C2. $V_{\text{sig}}$ is the output voltage of the pixel, and $V_{\text{con}}$ is the DC offset we would like to apply to the voltage output of the DDS.

During the hold operation, the pixel output is now its reset voltage, $V_{\text{reset}}$. If we model the amplifier as a device that multiplies the difference of its inputs by its open loop gain, $A$ and call the minus node of the amplifier $V_{\text{input}}$, we can write:

$$V_{\text{out}} = -A(V_{\text{ref}} - V_{\text{input}}) \quad (4.47)$$

The charge equations for capacitors C1 and C2 are now:

$$Q_{1\text{old}} = C1(V_{\text{input}} - V_{\text{reset}}) \quad (4.48)$$

$$Q_{2\text{old}} = C2(V_{\text{input}} - V_{\text{out}}) \quad (4.49)$$

Since the charge at the input of the amplifier is conserved,

$$Q_{1\text{sample}} + Q_{2\text{sample}} = Q_{1\text{old}} + Q_{2\text{old}} \quad (4.50)$$

$$C1(V_{\text{ref}} - V_{\text{sig}}) + C2(V_{\text{ref}} - V_{\text{con}}) = C1(V_{\text{input}} - V_{\text{reset}}) + C2(V_{\text{input}} - V_{\text{out}}) \quad (4.51)$$

Solving for $V_{\text{ref}}$:

$$V_{\text{ref}} = \frac{C1(V_{\text{sig}} + V_{\text{input}} - V_{\text{reset}}) + C2(V_{\text{input}} - V_{\text{out}} + V_{\text{con}})}{C1 + C2} \quad (4.52)$$

Since C1 and C2 are set to the same value, C1 and C2 can be replaced with C:

$$V_{\text{ref}} = \frac{C(V_{\text{sig}} + V_{\text{input}} - V_{\text{reset}} + V_{\text{input}} - V_{\text{out}} + V_{\text{con}})}{2C} \quad (4.53)$$

$$V_{\text{ref}} = \frac{(V_{\text{sig}} + V_{\text{input}} - V_{\text{reset}} - V_{\text{out}} + V_{\text{con}})}{2} \quad (4.54)$$

Plugging this back into equation (4.47),
\[ V_{\text{out}} = -A \left( \frac{V_{\text{sig}} + 2V_{\text{input}} - V_{\text{reset}} - V_{\text{out}} + V_{\text{con}}}{2} - V_{\text{input}} \right) \]  

\[ V_{\text{out}} \left( 1 - \frac{A}{2} \right) = -A \left( \frac{V_{\text{sig}} - V_{\text{reset}} + V_{\text{con}}}{2} \right) \]

If \( A \gg 2 \),

\[ V_{\text{out}} = V_{\text{sig}} - V_{\text{reset}} + V_{\text{con}} \]

Thus as long as the amplifier gain is much greater than 2, then the DDS output voltage will be the pixel output with the pixel reset of the next pixel subtracted off and a constant DC offset of \( V_{\text{con}} \). \( V_{\text{con}} \) is produced from off chip and will be used to tune the DC level of the DDS output voltage.

Depending on which part of the dynamic range the output voltage to the DDS is in, the DC open loop of the amplifier varies between 2273 to 4385, which is much greater than 2. The bandwidth of the amplifier is around 128MHz. The open loop gain for different output DC voltage levels is shown in Figure 4.4

Figure 4.4: Open loop gain of DDS amplifier implemented as a cascoded common source. The amplifier is biased to consume 3\( \mu \)A of current.
Figure 4.5: Closed Loop gain of the DDS stage operating under normal conditions. The closed loop gain is very close to unity across its full dynamic range.

Noise simulations yielded a worst integrated input referred noise of 329.3µV for a DC output voltage of 2.65V.

The closed loop gain was also simulated to make sure that the DDS had a linear output. Ideally, the closed loop gain should be as close to unity as possible. The output pixel voltages from pixel simulations ranged from about 0.9V to 2.9V. With a reset around 1V, this means that the output level of the DDS stage would range from 0.65V to 2.65V if the DC offset voltage, $V_{\text{con}}$, is 0.75V. For the closed loop gain simulations, the pixel output was simulated by varying a voltage between 0.9V and 2.9V. During the hold phase of the DDS, the pixel output was brought to 1V, the expected reset voltage of a pixel. The output of the DDS would then range from 0.65V to 2.65V, and the gain for each point was calculated by subtracting the DC offset voltage, $V_{\text{con}}$ from each DDS output voltage and dividing it by the corresponding input voltage. The plot of gain over the full input range is shown in Figure 4.5.
**Section 4.3.2: Sample / Hold Stage**

The gain of the Sample / Hold stage must be very close to 1 because the inter-stage gain is the product of the gain of the Sample / Hold stage and the MDAC stage. A typical sample / hold scheme was used [87]. A single capacitor both samples and acts as the feedback capacitor to make the circuit immune to capacitor mismatch. An extra capacitor was added to ground to minimize the effects of charge injection. The circuit implementation is shown in Figure 4.6.

For mathematical analysis, the node at the input of the amplifier will be called $V_c$. During the sample phase, the amplifier is put in unity feedback, so the output voltage is equal to approximately $V_{ref}$. Since $V_{ref}$ only appears in the equations when the amplifier is in unity feedback, the small deviation from finite gain will be ignored because it will be the same whenever it is in unity feedback. The charge across the capacitors are:

$$Q_1 = C_1(V_{ref} - V_{sig}) \quad (4.58)$$
$$Q_2 = C_2(V_{ref} - 0) \quad (4.59)$$

During the hold phase, the output of the amplifier can be modeled as:

$$V_{out} = -A(V_{ref} - V_c) \quad (4.60)$$

Where $A$ is the open loop gain of the amplifier. The charge equations during the hold phase are now

$$Q_1 = C_1(V_c - V_{out}) \quad (4.61)$$
$$Q_2 = C_2(V_c - 0) \quad (4.62)$$

Equating the sum of the charges from the two phases:

$$Q_1 + Q_2 = Q_1 + Q_2$$
$$C_1(V_{ref} - V_{sig}) + C_2(V_{ref}) = C_1(V_c - V_{out}) + C_2(V_c) \quad (4.64)$$

Solving for $V_c$,
\[
V_c = \frac{C1(V_{ref} - V_{sig} + V_{out}) + C2(V_{ref})}{C1 + C2}
\]  
(4.65)

Plugging equation (4.65) into (4.60),

\[
V_{out} = -A\left(V_{ref} - \frac{C1(V_{ref} - V_{sig} + V_{out}) + C2(V_{ref})}{C1 + C2}\right)
\]  
(4.66)

\[
V_{out} = A\left(\frac{C1(-V_{sig} + V_{out})}{C1 + C2}\right)
\]  
(4.67)

\[
V_{out}(1 - \frac{A(C1)}{C1 + C2}) = A\left(\frac{C1(-V_{sig})}{C1 + C2}\right)
\]  
(4.68)

Since \(C1\) and \(C2\) are approximately equal, then if \(A>>2\)

\[
V_{out}\left(-\frac{A(C1)}{C1 + C2}\right) = A\left(\frac{C1(-V_{sig})}{C1 + C2}\right)
\]  
(4.69)

\[
V_{out} = V_{sig}
\]  
(4.70)

The gain error is approximately equal to the inverse of the gain.

The constraints for the amplifier are high gain and high dynamic range while minimizing area and power. A standard two stage op-amp was chosen because of it could achieve high gain with a high dynamic range using the common source amplifier in the second stage. The amplifier used is a modified version of the two stage amplifier found in Baker that connects the feedback capacitor via a buffered output [88]. This reduces the size of the feedback capacitor needed to stabilize the high gain amplifier.

The amplifier was modified by adding cascodes in the first stage for high gain so the dynamic range is not compromised. It was further modified by adding a second buffer using a PMOS common drain architecture to reduce noise. The second buffer also has its own smaller capacitor. The gain of the amplifier was high enough with a range between 1.6 million to 2.38 million across its dynamic range (see Figure 4.8). Across the dynamic range, the integrated input noise could be as high as 382.1\(\mu\)V and as low as 166.1\(\mu\)V. The bandwidth of the amplifier is 160MHz. Figure 4.7 shows the amplifier design used in the Sample / Hold stage.

The current biases were generated off a 1\(\mu\)A current bias coming from off chip that is mirrored and amplified. \(V_{bias\_opamp}\) is biased with 12\(\mu\)A, \(V_{b\_n}\) and \(V_{b\_p}\) are biased with 6\(\mu\)A, \(V_{bias\_opamp2}\) is
biased with 10µA, vbias_opamp3 is biased with 8µA, and vbias_opamp4 is biased with 8µA. In total, the amplifier consumes 38µA.

Figure 4.6: Circuit implementation of the Sample / Hold stage. A shows the overall circuit with the switches, B shows the clock waveforms that control the switches, C shows the circuit during the sample phase, and D shows the circuit during the hold phase. E shows the layout implementation of the Sample / Hold stage. Capacitors in the amplifier were implemented using DMIM capacitors; capacitors C1 and C2 were implemented with poly-poly capacitors to minimize parasitic capacitances from metal lines.
Figure 4.7: Amplifier design used for the Sample / Hold Stage and MDAC stage. Vbias_opamp, vbias_opamp2, vbias_opamp3 and vbias_opamp4 are current biases; vb_n and vb_p are cascode biases. The amplifier uses a cascoded OTA in the first stage for high gain, and a common source in the second stage. Two common drain buffers help reduce the capacitance needed to stabilize the amplifier and reduce noise.
**Figure 4.8**: Open loop amplifier gain at different parts of the output dynamic range. It shows DC gain well into the millions for DC output ranges from 0.35V to 2.95V, which ensures a closed loop gain very close to 1. The bandwidth of the amplifier is 160MHz.
Section 4.3.3: Multiplying Digital-to-Analog Converter (MDAC)

The MDAC subtracts the DAC voltage reference from the Sample / Hold stage output and multiplies the result by the inter-stage gain of 4. As discussed in Section 4.2, the inter-stage gain should be very precise to avoid distortion at the ADC output. To achieve precise inter-stage gain, a circuit typically used for 1.5 bit per stage pipeline ADC was implemented [66]. The circuit typically used samples the input voltage twice and outputs it across the same sampling capacitor to achieve a gain of two that is immune to capacitor mismatch. To achieve a gain of 4, the same idea was used, but the input is sampled 4 times in order to achieve a gain of four. The overall circuit is shown in Figure 4.9, and each phase in the circuit will be described in detail.

![Circuit Diagram](image)

**Figure 4.9:** A shows an overall circuit diagram of MDAC circuit. Vsig is the signal from the Sample / Hold stage, Vref is the DAC voltage reference, and Vmid is constant voltage bias at 1.65V. Vc is the voltage at the minus terminal of the Amplifier. S<0> to S<7> are control signals for the switches (high indicates switch is closed). C1 and C2 are chosen to be the same so the amplifier does not saturate during operation. B shows the layout of the MDAC stage.
Figure 4.10: Phase 1 of the MDAC stage. The voltage from the S / H stage (Vsig) is sampled.

In phase 1, S<2>, S<3>, S<6> and S<5> are closed, resulting in the circuit shown in Figure 4.10.

During phase one, the S / H stage output is sampled. The amplifier is in unity feedback, but since Vmid also appears as a bias voltage elsewhere in the circuit, we will consider the error from finite gain. For an amplifier in unity feedback with gain A, the output voltage is given by

\[ V_{out} = -A(V_+ - V_-) = -A(V_+ - V_{out}) \]  \hspace{1cm} (4.71)

\[ V_{out} = \frac{A(V_+)}{1 - A} = \frac{A}{A - 1} V_+ \]  \hspace{1cm} (4.72)

Since the amplifier is in unity feedback, the charge across the capacitors is:

\[ Q_1 = C_1 \left( \frac{A}{A - 1} V_{mid} - V_{sig} \right) \]  \hspace{1cm} (4.73)

\[ Q_2 = C_2 \left( \frac{A}{A - 1} V_{mid} - V_{mid} \right) = C_2 \left( \frac{1}{A - 1} V_{mid} \right) \]  \hspace{1cm} (4.74)
Figure 4.11: Phase 2 of the MDAC stage stores the difference between the sampled signal and the DAC voltage reference on capacitor C2.

In phase 2, switches S<0>, S<3> and S<4> are closed.

The reference voltage is sampled, and the charge stored across C2 involves the difference between the S/H signal and the DAC reference voltage.

\[ Q_{12} = C_1(V_c - V_{ref}) \]  
\[ Q_{22} = C_2(V_{out} - V_c) \]  
\[ V_{out} = -A(V_{mid} - V_c) \]

The sum of \( Q1 \) and \( Q2 \) should be conserved, so the sum from phase 1 should equal the sum of the charges in phase 2.

\[ Q_{11} + Q_{21} = Q_{12} + Q_{22} \]  
\[ C_1(\frac{A}{A-1}V_{mid} - V_{sig}) + C_2\left(\frac{1}{A-1}V_{mid}\right) = C_1(V_c - V_{ref}) + C_2(V_{out} - V_c) \]

Solving for \( V_c \):
\[
V_c = \frac{C_1(V_{mid} - V_{sig} + V_{ref}) - C_2\left(-\frac{1}{A-1}V_{mid} + V_{out}\right)}{C_1 - C_2}
\]  

(4.80)

Plugging equation (4.22) into (4.77),

\[
V_{out} = -A\left(V_{mid} - \frac{C_1(V_{mid} - V_{sig} + V_{ref}) - C_2\left(-\frac{1}{A-1}V_{mid} + V_{out}\right)}{C_1 - C_2}\right)
\]  

(4.81)

\[
V_{out} = \left(\frac{C_1 - C_2}{A(C_2) + C_1} - C_2\right)\left(A(C_1)(-V_{sig} + V_{ref}) + A(C_2)((1 + \frac{1}{A-1})V_{mid})\right)
\]  

(4.82)

\[
V_{out} = \left(\frac{A}{(A-1)C_2 + C_1}\right)\left(C_1(-V_{sig} + V_{ref}) + C_2\left(1 + \frac{1}{A-1}\right)V_{mid}\right) + V_{out}
\]  

(4.83)

Now we can solve for \(V_c\) using equation (4.77),

\[
\left(\frac{A}{(A-1)C_2 + C_1}\right)\left(C_1(-V_{sig} + V_{ref}) + C_2\left(1 + \frac{1}{A-1}\right)V_{mid}\right) = -A(V_{mid} - V_c)
\]  

(4.84)

\[
V_c = \left(\frac{1}{(A-1)C_2 + C_1}\right)\left(C_1(-V_{sig} + V_{ref}) + C_2\left(1 + \frac{1}{A-1}\right)V_{mid}\right) + V_{mid}
\]  

(4.85)

Now we know the charge across \(Q_2\):

\[
Q_{2_2} = C_2(V_{out} - V_c)
\]  

(4.86)

\[
= C_2\left(\frac{1}{(A-1)C_2 + C_1}\right)\left(C_1(-V_{sig} + V_{ref}) + C_2\left(1 + \frac{1}{A-1}\right)V_{mid}\right) + V_{mid}
\]  

(4.87)

If we assume \(A >> 2\) and \(A(C_2) >> C_1\), we can greatly simplify this equation and further analysis:

\[
Q_{2_2} = C_1(-V_{sig} + V_{ref})
\]  

(4.88)
Figure 4.12: Phase 3 of the MDAC stage samples the S / H output again while storing the previous difference on C2.

In phase 3, switches S<0>, S<2> and S<4> are closed. The negative terminal on C2 is left floating so that the charge across the capacitor is conserved. C1 samples the S / H output as in phase 1.

\[
Q_{1.3} = C1 \left( \frac{A}{A-1} V_{\text{mid}} - V_{\text{sig}} \right)
\]

(4.89)

Using our simplifying assumptions for large A,

\[
Q_{1.3} = C1 (V_{\text{mid}} - V_{\text{sig}})
\]

(4.90)
Figure 4.13: Phase 4 of the MDAC stage stores the difference between the sampled signal and the DAC voltage reference on capacitor C2 along with the previous difference from phase 2.

\[ Q_{23} = C_1(-V_{\text{sig}} + V_{\text{ref}}) \]  \hspace{1cm} (4.91)

The charge equations during phase 4 are the same as in phase 2,

\[ Q_{14} = C_1(V_c - V_{\text{ref}}) \] \hspace{1cm} (4.92)

\[ Q_{24} = C_2(V_{\text{out}} - V_c) \] \hspace{1cm} (4.93)

Equating the sum of the charges from phase 3 and phase 4

\[ Q_{13} + Q_{23} = Q_{14} + Q_{24} \] \hspace{1cm} (4.94)

\[ C_1(V_{\text{mid}} - V_{\text{sig}}) + C_1(-V_{\text{sig}} + V_{\text{ref}}) = C_1(V_c - V_{\text{ref}}) + C_2(V_{\text{out}} - V_c) \] \hspace{1cm} (4.95)

Solving for \( V_c \),

\[ V_c = \frac{C_1(V_{\text{mid}} + 2V_{\text{ref}} - 2V_{\text{sig}}) - C_2(V_{\text{out}})}{C_1 - C_2} \] \hspace{1cm} (4.96)

Now the output voltage can be solved.
\[ V_{\text{out}} = -A(V_{\text{mid}} - V_c) \quad (4.97) \]

\[ V_{\text{out}} = -A \left( V_{\text{mid}} - \frac{C_1(V_{\text{mid}} + 2V_{\text{ref}} - 2V_{\text{sig}}) - C_2(V_{\text{out}})}{C_1 - C_2} \right) \quad (4.98) \]

\[ V_{\text{out}} = \left( \frac{C_1 - C_2}{C_1 + (A-1)(C_2)} \right) \left( -A \left( -\frac{C_1(2V_{\text{ref}} - 2V_{\text{sig}}) + C_2(V_{\text{mid}})}{C_1 - C_2} \right) \right) \quad (4.99) \]

Assuming \( C_2(A-1) \gg C_1 \)

\[ V_{\text{out}} = \left( \frac{C_1(2V_{\text{ref}} - 2V_{\text{sig}})}{C_2} \right) + V_{\text{mid}} \quad (4.100) \]

Plugging this back into (4.97) to solve for \( V_c \),

\[ \left( \frac{C_1(2V_{\text{ref}} - 2V_{\text{sig}})}{C_2} \right) + V_{\text{mid}} = -A(V_{\text{mid}} - V_c) \quad (4.101) \]

\[ V_c = \left( \frac{C_1(2V_{\text{ref}} - 2V_{\text{sig}})}{A(C_2)} \right) + \frac{V_{\text{mid}}(1+A)}{A} \approx V_{\text{mid}} \quad (4.102) \]

Then the charge across \( C_2 \) can be rewritten as

\[ Q_2 = C_2 \left( \frac{C_1(2V_{\text{ref}} - 2V_{\text{sig}})}{C_2} \right) + V_{\text{mid}} - V_{\text{mid}} = C_1(2V_{\text{ref}} - 2V_{\text{sig}}) \quad (4.103) \]
Figure 4.14: Phase 5 of the MDAC stage samples the S/H output again while storing the previous two differences on C2.

Phase 5 is the same as phase 3 where the Sample / Hold output voltage is sampled again and the charge on C2 is conserved by floating the negative terminal of the capacitor.

\[ Q_{15} = C_1(V_{mid} - V_{sig}) \]  \hspace{1cm} (4.104)  

\[ Q_{25} = C_1(-2V_{ref} + 2V_{sig}) \]  \hspace{1cm} (4.105)
Figure 4.15: Phase 6 of the MDAC stage stores the difference between the sampled signal and the DAC voltage reference on capacitor C2 along with the previous 2 differences from previous phases.

Phase 6 is the same as phase 4 and is adding the difference between the sample / hold output and the DAC voltage reference to the differences accumulated from previous phases and storing it on C2.

\[ Q_{16} = C_1 (V_c - V_{ref}) \]  \hspace{1cm} (4.106)

\[ Q_{26} = C_2 (V_{out} - V_c) \]  \hspace{1cm} (4.107)

The same process to calculate \( V_{out} \) and \( V_c \) will be used here as in phase 4. First the sum of the charges from phase 5 is equated to the sum of charges in phase 6.

\[ Q_{15} + Q_{25} = Q_{16} + Q_{26} \]  \hspace{1cm} (4.108)

\[ C_1 (V_{mid} - V_{sig}) + C_1 (-2V_{sig} + 2V_{ref}) = C_1 (V_c - V_{ref}) + C_2 (V_{out} - V_c) \]  \hspace{1cm} (4.109)

Solving for \( V_c \),

\[ V_c = \frac{C_1 (V_{mid} + 3V_{ref} - 3V_{sig}) - C_2 (V_{out})}{C_1 - C_2} \]  \hspace{1cm} (4.110)

Now the output voltage can be solved
\[ V_{out} = -A(V_{mid} - V_c) \]  
(4.111)

\[ V_{out} = -A \left( V_{mid} - \frac{C1(V_{mid} + 3V_{ref} - 3V_{sig}) - C2(V_{out})}{C1 - C2} \right) \]  
(4.112)

\[ V_{out} = \left( \frac{C1 - C2}{C1 + (A-1)(C2)} \right) \left( -A \left( - \frac{C1(3V_{ref} - 3V_{sig}) + C2(V_{mid})}{C1 - C2} \right) \right) \]  
(4.113)

Assuming \( C2(A-1) \gg C1 \)

\[ V_{out} = \left( \frac{C1(3V_{ref} - 3V_{sig})}{C2} \right) + V_{mid} \]  
(4.114)

Plugging this back into (4.111) to solve for \( V_c \),

\[ \left( \frac{C1(3V_{ref} - 3V_{sig})}{C2} \right) + V_{mid} = -A(V_{mid} - V_c) \]  
(4.115)

\[ V_c = \left( \frac{C1(3V_{ref} - 3V_{sig})}{A(C2)} + \frac{V_{mid}(1 + A)}{A} \right) \approx V_{mid} \]  
(4.116)

Then the charge across \( C2 \) can be rewritten as

\[ Q_{2c} = C2 \left( \left( \frac{C1(3V_{ref} - 3V_{sig})}{C2} \right) + V_{mid} - V_{mid} \right) = C1(3V_{ref} - 3V_{sig}) \]  
(4.117)

**Figure 4.16:** Phase 7 of the MDAC stage samples the S/H output again while storing the previous three differences on \( C2 \).
Phase 7 is the same as phase 3 and 5. The Sample / Hold output voltage is sampled again and the charge on 
C2 is conserved by floating the negative terminal of the capacitor.

\[ Q_{17} = C1(V_{mid} - V_{sig}) \]  \hspace{1cm} (4.118) 

\[ Q_{27} = C1(-3V_{ref} + 3V_{sig}) \]  \hspace{1cm} (4.119) 

Figure 4.17: Phase 8 of the MDAC stage stores the difference between the sampled signal and the DAC 
voltage reference on capacitor C2 along with the previous 3 differences from previous phases.

Phase 8 is also identical to phase 4 and 6. The exact same mathematical process is used as in 4 and 6. It is 
clear from following the math in phase 4 and 6 that nothing changes except the coefficient on \( V_{ref} \) and \( V_{sig} \).

The final result for the output voltage and charge across capacitors are:

\[ V_{out} = \left( \frac{C1(4V_{ref} - 4V_{sig})}{C2} \right) + V_{mid} \]  \hspace{1cm} (4.120) 

\[ Q_{18} = C1(V_{mid} - V_{ref}) \]  \hspace{1cm} (4.121) 

\[ Q_{28} = C1(4V_{ref} - 4V_{sig}) \]  \hspace{1cm} (4.122)
Equation (4.120) is almost the desired result of the MDAC; however, it still depends on the ratio between C1 and C2. It would be desirable to simply transfer the charge across C2 to C1; however, that cannot be done in one step because there is still charge on Q1.

In phase 9, the charge across C1 is dumped while the negative terminal of C2 is left floating to conserve the charge on it. Switches S<2>, S<4> and S<7> are closed.

Figure 4.18: Phase 9 of the MDAC stage makes the charge across C1 approximately 0 and stores the charge from previous phases on C2 by floating the negative terminal of C2.

\[
Q_{1} = C_{1} \left( V_{\text{mid}} - \frac{A}{A-1} V_{\text{mid}} \right) \approx 0 \quad (4.123)
\]

\[
Q_{2} = C_{1} \left( 4V_{\text{ref}} - 4V_{\text{sig}} \right) \quad (4.124)
\]
Figure 4.19: Phase 10 of the MDAC stage transfers the charge to $C_1$, making the output voltage the desired MDAC output and immune to capacitor mismatch.

In phase 10, all the charge is transferred to $C_1$, and the resulting output voltage is now immune to capacitor mismatch. Switches $S<1>$, $S<3>$ and $S<5>$ are closed. In this phase, the charge across $C_2$ is approximately zero, which ensures that all charge is transferred to $C_1$.

\[ Q_{1_{10}} = C_1(V_c - V_{out}) \]  

(4.125)

\[ Q_{2_{10}} = C_2 \left( V_{mid} - \frac{A}{A-1}V_{mid} \right) \approx 0 \]  

(4.126)

We can write another equation for $V_{out}$ with our model of the amplifier:

\[ V_{out} = -A(V_{mid} - V_c) \]  

(4.127)

Using conservation of charge, the sum of the charges from phase 9 is equal to the sum of the charges from phase 10.

\[ Q_{1_9} + Q_{2_9} = Q_{1_{10}} + Q_{2_{10}} \]  

(4.128)

\[ 0 + C_1(4V_{ref} - 4V_{sig}) = C_1(V_c - V_{out}) + 0 \]  

(4.129)
\[ V_c = 4V_{ref} - 4V_{sig} + V_{out} \quad (4.130) \]

Plugging equation (4.22) into equation (4.127),

\[ V_{out} = -A(V_{mid} - (4V_{ref} - 4V_{sig} + V_{out})) \quad (4.131) \]

\[ V_{out} = -\frac{A}{1 - A}(4(V_{sig} - V_{ref}) + V_{mid}) \quad (4.132) \]

Since we assumed \( A \gg 1 \),

\[ V_{out} = 4(V_{sig} - V_{ref}) + V_{mid} \quad (4.133) \]

Equation (4.133) is the final result of the MDAC stage and achieves an inter-stage gain of 4 that does not depend on capacitor matching but instead does it in time. The DC offset of \( V_{mid} \) is desirable so that the MDAC output is centered in between ground and the supply voltage, and as was shown in section 3.1, the effects of the DC offset cancels out. The only assumption in these equations is that the gain of the amplifier is high. The dynamic range of the amplifier needs to be higher than the comparator references, thus the same amplifier used in the Sample / Hold circuit was used because it satisfies both of these constraints. The clock waveforms for \( S<0> \) to \( S<7> \) are shown in Figure 4.20.

**Figure 4.20:** Clock waveforms for signals controlling the switches in the MDAC stage. 4 cycles are shown here, which corresponds to one complete digitization by the ADC.
Section 4.3.4: Comparator

The comparator needs a high input dynamic range since the comparator references go from 0.4V to 2.9V. Additionally, the kickback noise needs to be low. The speed of the comparator does not need to be high, and power should be minimized. Thus a latched comparator was used for low power, and a pre-amplifier stage was added to increase the input dynamic range and reduce comparator kickback noise. The pre-amplifier stage does not need to provide any gain because the latched comparator design has positive feedback and high gain.

Figure 4.21: A shows the pre-amplifier stage for the latched comparator. It achieves high input dynamic range and reduces comparator kickback noise. Vp_bias is biased with 10µA. B shows the layout of the whole comparator (pre-amplifier and latched comparator).
Figure 4.22: Open loop of Comparator Pre-amplifier at different DC input levels. The highest DC gain is 16.4 and the lowest DC gain is 0.698.

The pre-amplifier used is shown in Figure 4.21 and is simply a modified five transistor OTA. The OTA was implemented with a PMOS input pair and PMOS current source. An NMOS input pair was added to increase the input dynamic range. A NMOS switch was added at the bottom to turn off the pre-amplifier when the comparator is not being used to save power. The gain characteristics are shown in Figure 4.22.

The latched comparator design used did not use any special modifications and the design was found in [89]. Minimum sized transistors were used to minimize area and power consumption. Since only one of the outputs would be used in the circuit, only one latch was implemented for one of the outputs of the comparator. Figure 4.23 shows a transistor schematic of the latched comparator. In order to characterize noise of the whole comparator including the pre-amplifier and the latched comparator, transient noise simulations were run because it is a highly non-linear system. Input referred noise was calculated from simulation by first measuring the offset at each comparison level and then inputting an input with a small deviation from the offset (zero) level. The number of zeros was counted and the z-score was used to calculate the standard deviation. 781µV is the worst case at $V_{ref} = 0.4V$. In the best case the noise is 123µV at $V_{ref} = 1.4V$. The latched comparator was controlled using two non-overlapping clock signals.
Figure 4.23: Schematic of latched comparator design. The clock signals are low when the comparator is not used.

The average power consumption of the comparator is estimated to be 9.504µA. The pre-amplifier is biased with 10µA and has a duty cycle of:

\[
\text{duty cycle} = \frac{\left(\frac{5 \text{ cycles}}{\text{row}}\right) \left(6 \text{ comparisons}\right) \left(\frac{50 \text{ns}}{\text{comparison}}\right)}{20.833 \mu\text{s per row}} \approx 0.072
\]

(4.134)

Therefore the power consumption from the pre-amplifier is approximately 0.72µA. If we use a conservative estimate of 100µA current draw during the regeneration period of the latched comparator, then using the same duty cycle yields 7.2µA. Therefore an estimate of the total average power consumption of the comparator is 7.92µA.
Section 4.3.5: Comparator and Multiplying Digital-to-Analog Converter Voltage References

An array of switches was used to implement the different comparator and MDAC voltage references. When the switches switch, they draw current because node in the column ADC is charged to the previous voltage reference. Thus in order to minimize current draw, the capacitance of the voltage reference node in each ADC was minimized. By using a minimum sized transmission gate, capacitance of the voltage reference node is minimized. Because the array of switches draws current from the voltage references, buffers were designed to buffer the voltage lines and will be discussed in Section: 4.3.8.1.

![Switch Diagram]

Figure 4.24: Implementation of array of switches to control the comparator and MDAC voltage references. Minimum sized transmission gates were used as switches as shown at the top of the Figure to minimize the capacitance. Switch<sub>x</sub> refers to the output of the shift register counter discussed in Section 4.3.6.
Section 4.3.6: Digital Logic

The digital logic in each column should implement the equations for the ADC algorithm in Section 4.2. A block diagram of the circuit implementation of the digital logic is shown in Figure 4.25. An asynchronous latch acts as a state machine that keeps track if the comparator output changes. At the beginning of each cycle, the state machine is reset to the “count” state, which allows the counter and shift register counter to increment. Once the comparator result changes, the state machine goes to the “pause” state where the counters no longer increment and the value is held. The shift register counter values control the comparator and MDAC DAC voltage references. The lowest count represents the lowest comparator and MDAC voltage reference. Thus as the count increases, the comparator reference is stepped up until the comparator reference passes the Sample / Hold output voltage. Since each digitization is 2.8074 bits or 7 levels, it can either be stored as 3 bits or in a 7-bit shift register. A 7-bit shift register is a convenient way to control the DAC switches, so it is stored that way for controlling the comparator and MDAC voltage references. For the actual digital value, it is stored as a signed number (2’s complement) between -3 and 3. This way it is easy to manipulate.

After the comparisons are done the value should be multiplied by a power of the inter-stage gain. Since the inter-stage gain is 4, this corresponds to shifting right by multiples of 2. This is essentially an 11-bit shift register that only shifts by 2 instead of one, or equivalently one 5-bit shift register and one 6-bit register. It needs to be 11-bits because the greatest multiplication is by 256, which corresponds to a shift 8. Since the original digitization can occupy up to 3 bits, this will be shifted up to the 11th bit. The number of shifts is controlled from the digital clock generator that is not in the column. Since the first digitization always needs to be multiplied by 256, the second digitization always needs to be multiplied by 64, the third by 16, the fourth by 4, and the fifth by 1, the number of shifts follows a pattern. The result from each cycle needs to be summed together, and this is handled by an 11-bit accumulator (adder and register). Finally, after the accumulation is complete, the data is transferred to an 11-bit shift register that shifts all the ADC outputs out serially. The output is 11-bits to handle saturation cases to ensure the result never overflows. This can be seen easily by looking at the maximum and minimum values the ADC can output. The maximum values is if every digitization gives a +3,
\[ 3(4^4 + 4^3 + 4^2 + 4^1 + 4^0) = 1023 \]  

(4.135)

The minimum value is if every digitization gives a 3,

\[ -3(4^4 + 4^3 + 4^2 + 4^1 + 4^0) = -1023 \]  

(4.136)

An 11-bit value encoded in 2’s complement can handle values between -1024 and 1023, so with 11-bits, the accumulator will never overflow.

**Figure 4.25:** Block diagram of implementation of the ADC digital logic that exists in every column of the ADC.
Section 4.3.7: Digital Clock Generator

Digital clocks that are shared across the array are generated in one part of the chip and distributed across the array. These clocks include the signals that control the DDS stage, Sample / Hold stage, MDAC stage, comparator, digital logic, and pixel control signals. In addition, it also produces signals needed for readout such as frame valid and line valid signals. A frame valid signal being high indicates that the frame is still valid. Once it goes low, it signifies the end of a frame. The line valid signal being high indicates that the data coming out is all data from a particular row, and once it goes low it signifies the end of a row. The inputs to the digital clock generator are the desired exposure time, the external reset signal, and the master clock. Since this block of digital is large and will need buffering and precise timing considerations to avoid

Figure 4.26: Layout generated by Cadence Encounter of the Digital Clock Generator.
timing violations for registers, it was generated using standard cells. A VHDL description of the circuit was written and imported into Synopsys, which was used as the synthesis tool. Cadence encounter was used as the place and route tool and generated the layout. For simulation with the ADC, the Verilog description from cadence encounter with timing information was used for speed purposes. A transistor level simulation was also done with just the digital clock generator by itself to ensure correct operation.

Before the array, the digitally generated clock signals were buffered by appropriately sized inverters to drive the line. The line was modeled with an RC transmission line using extracted parameters to extract the appropriately sized buffers. The width of the lines was carefully matched with the current drive of the buffer to avoid electro migration.

Section 4.3.8: Other Supporting Circuitry

Section: 4.3.8.1 Voltage Reference Buffers

Since the comparator and MDAC DAC voltage references were implemented as switch arrays, they need to be buffered so that the voltage settles before the comparison or MDAC operation occurs. The buffers for all the voltages are stabilized by an off chip 1μF capacitor. Since the voltage references range from 0.15V to 3.15V, different buffer designs were used depending on the voltage range. For the lower buffer voltage references (0.15V, 0.4V, 0.65V), a flipped 5 transistor OTA was used for a first stage, a common source was used in the second stage, and a third buffer stage was added for high current drive. For both the comparator and MDAC stages, there was about 100ns for the voltage reference signal to settle before it was used; Figure 4.27c shows that the signal settles nicely in that time. Figure 4.27 describes the schematic, gain characteristics and layout implementation of the buffer as well.

For the middle range voltages (0.9V, 1.15V, 1.4V, 1.65V, 1.9V, 2.15V, 2.4V), a similar structure was used. However, it was found that the circuit was faster without the extra buffer stage, so that was taken out. The regular 5 transistor OTA was used in the first stage and a common source was used in the second stage. Figure 4.28 shows the schematic, gain characteristics, settling time characteristics, and layout implementation of the middle range voltage buffers.

The higher range voltages (2.65V, 2.9V, 3.15V) also used a typical 5 transistor OTA in the first stage and a common source amplifier in the second stage. For the output stage, a common drain was used,
but the voltage reference was taken from the output of the second stage. It was found that the settling time characteristics were better if the first stage output was used instead of a constant voltage reference. At the highest voltage reference (3.15V), only a gain of about 2000 was achievable because the reference voltage is close to the supply voltage (3.3V). The output stage transistor that connects to the supply voltage was sized very wide to put the transistor in saturation. **Figure 4.29** shows the schematic, gain characteristics, settling time characteristics, and layout implementation of the high end voltage buffers.
Figure 4.27: Buffer for lower end voltage range of Comparator Reference and MDAC DAC references. It buffers 0.15V, 0.4V and 0.65V. The circuit diagram is shown in A, the gain and settling time characteristics are shown in B and C respectively for the different buffer voltages and the layout implementation is shown in D.
Figure 4.28: Buffer for middle voltage range of Comparator Reference and MDAC DAC references. It buffers 0.9V, 1.15V, 1.4V, 1.65V, 1.9V, 2.15V and 2.4V. The circuit diagram is shown in A, the gain and settling time characteristics are shown in B and C respectively for the different buffer voltages and the layout implementation is shown in D.
Figure 4.29: Buffer for high end voltage range of Comparator Reference and MDAC DAC references. It buffers 2.65V, 2.9V, and 3.15V. The circuit diagram is shown in A, the gain and settling time characteristics are shown in B and C respectively for the different buffer voltages and the layout implementation is shown in D.
Section: 4.3.8.2 Bias Generators

The voltage references for the comparator and MDAC voltage references were generated using a resistor ladder. It consists of 66 10kΩ unit resistors in series. For layout purposes, each 10kΩ resistor was split into two 5kΩ resistors so resistors could be laid out symmetrically for matching purposes. The voltage at the very top of the resistor ladder is nominally 3.3V, but it is supplied from off chip and can be adjusted if desired. Between each of the 66 resistors, there is a 0.05V drop, and the appropriate voltages are tapped from the resistor ladder by the buffers in Section: 4.3.8.1. Layout strategy is shown in Figure 4.30.

Current biases were generated on chip for the amplifiers using a 1μA off chip current reference. A PMOS and NMOS version of the 1μA current was generated (see Figure 4.31A) from a circuit found in [85]. A number of these in parallel were used as the current source to a diode connected transistor to produce the voltage references for the amplifiers. The DDS bias voltages are generated in the same way as the pixel voltage biases [85]. The rest of the voltage biases are generated using diode connected transistors, with cascode biases having an additional transistor that simulate the voltage drop from the input transistor. Figure 4.31 depicts the bias generation circuits.

Figure 4.30: Layout implementation of resistor ladder. A shows the layout and B depicts how the resistors are connected to reduce mismatch. R1A and R1B are both 5kΩ resistors that combine to make a unit 10kΩ resistor. The two 5kΩ resistors that make up a unit resistor are all equidistant from the center of the center of the resistor ladder. The amount of metal wiring is also equalized because resistors that are close together are wired farther out (see R66A ,R66B in B).
Figure 4.31: Generation of voltage biases for amplifier circuits in the ADC. A shows how four biases (pbias, casp, vcasn, bias) are generated. These are used to generate all other biases. B shows the circuit used to create the biases for the DDS circuit; this is the same circuit type of circuit used to generate the pixel biases. C shows the generation of biases for the voltage buffers, and D shows the generation of biases for the MDAC and comparator circuits.
Section 4.4: ADC Verification Simulation Results

To verify correct operation of the ADC, an extracted view of 3 ADC’s using C+CC extraction (Capacitance and Coupling Capacitance) was used for simulation, and the output of the middle ADC was used. A Verilog description with timing information of the digital clocks from cadence encounter was used to drive buffers. The buffers connected to a transmission line model of the wiring so that the simulated ADC would be at the other end of the array from the buffer. R+C+CC (resistance and capacitance extraction) was not used because of unreasonable simulation times.

To test the resolution of the ADC, a full scale sine wave was input into the ADC to calculate the Effective Number of Bits (ENOB). For this simulation, a transient noise simulation was done where the simulator injects noise into the system according to device properties; this was done for noise frequencies from the sampling rate up to 200MHz. Because of long simulation times, 5 periods of the sine wave were simulated with the ADC sampling it 16 times. The data was then read into MATLAB for analysis.

In MATLAB, an FFT of the ADC output was taken, and the power within the frequency band corresponding to the sine wave frequency was compared to the power within all other frequency bands, and this was used to calculate ENOB, Signal-to-Noise and Distortion Ratio (SNDR) and Spurious-Free Dynamic Range (SFDR). A rectangular window was used. See Figure 4.32 for the FFT.

\[
SNDR = 10 \log_{10} \left( \frac{\text{Sine Wave Freq power}}{\text{All other Freq power}} \right) \quad (4.137)
\]

\[
ENOB = \frac{SNDR - 1.76}{6.02} \quad (4.138)
\]

\[
SFDR = 10 \log_{10} \left( \frac{\text{Sine Wave Freq power}}{\text{Next largest noise or harmonic power}} \right) \quad (4.139)
\]

The noise power from the ADC is the power at all other frequency powers. Thus, the total noise of the chip can be characterized and the expected SNDR at our expected output can be estimated.

\[
ADC \ Noise \ Power = \sum (\text{All other Freq power}) * \left( \frac{2V}{1024 \text{ levels}} \right)^2 \quad (4.140)
\]
Figure 4.32: Fast Fourier Transform of Output Sine Wave from ADC using a Rectangular window. The input sine wave was sampled 16 times over 5 periods. The output FFT was used to calculate the ENOB, SNDR and SFDR of the ADC.

\[ Total \ Noise \ Power = ADC \ Noise \ Power + Pixel \ Noise \ Power \]  \hspace{1cm} (4.141)

\[ System \ SNDR = 10 \log_{10}(\frac{Pixel \ Signal \ Power}{Total \ Noise \ Power}) \]  \hspace{1cm} (4.142)

The result of the calculations at the different fill factor estimates are shown in Table 4.1.
Table 4.1: Estimated System Performance for Different Fill Factor Estimates

<table>
<thead>
<tr>
<th>Silicide Block Area Fill Factor Estimate</th>
<th>Weighted QE estimation of fill factor</th>
<th>Max Fill Factor Estimate</th>
</tr>
</thead>
<tbody>
<tr>
<td>NE</td>
<td>782 electrons</td>
<td>950 electrons</td>
</tr>
<tr>
<td>Pixel Noise Power</td>
<td>3.5617µV²</td>
<td>4.1717µV²</td>
</tr>
<tr>
<td>ADC Noise Power</td>
<td>1.0634µV²</td>
<td>1.0634µV²</td>
</tr>
<tr>
<td>Total Noise Power</td>
<td>4.6251µV²</td>
<td>5.2351µV²</td>
</tr>
<tr>
<td>System SNDR</td>
<td>26.81dB</td>
<td>27.97dB</td>
</tr>
<tr>
<td>RMS Total Noise (LSBs)</td>
<td>1.10</td>
<td>1.17</td>
</tr>
</tbody>
</table>

To verify that the support circuitry, pixel circuitry and ADC circuitry are all synchronized correctly, a simulation with the pixel, ADC and supporting circuitry was done for a few levels to verify working logic. R+C+CC extractions of a 24x3 pixel array and C+CC extractions of a group of 3 ADCs were used. For the digitally generated clocks, the Verilog description with timing information was used for reasonable simulation time. The Verilog cells drove digital buffers that had transmission line loads for the various ADC clock lines. Schematic views were used for supporting circuitry. Previously supporting circuitry had been simulated with R+C+CC extracted views, but this made little difference in the simulation results. To save simulation time, the photodiode voltage was driven to a specified voltage instead of attaching a current source to it. Simulating the ADC for 16.67ms was unreasonable in terms of simulation time. When the pixel was selected, the photodiode voltage was allowed to float in order to allow the amplifier to drive the output to the correct voltage. For this simulation, different photodiode voltages were used across a group of 8 pixels (0.9V, 0.925V, 0.950V, 0.975V, 1V, 1.025V, 1.05V, 1.075V). Inherently the pixel output still has the pixel mismatch. The results of the simulation are shown in Figure 4.33.
Figure 4.33: Simulation of extracted pixel and ADC for a small array. The output looks fairly linear within the range of the ADC (-512 to 511). When the ADC goes beyond that, it becomes non-linear but is still monotonic.
Section 4.5: Chip Layout

Due to fabrication limitations, the chip size was limited to 8x9mm. The design kit came with pads designed for ESD protection, and these were used. Decoupling capacitors were added to the pads. In addition to the power rings in the pads themselves, custom power rings were added because of additional supply voltages. Separate digital and analog supplies and grounds were used, as well as a separate analog supply for the voltage buffer circuitry. In case the voltage buffers did not work properly, the voltage buffers could be turned off and the voltage references could be supplied from off chip. In addition, the power ring includes a separate digital supply for the pixel row select signal, which is at 1.8V. Analog and digital grounds are connected to the same substrate, but they are not connected by wiring on chip; digital and analog grounds will be connected off chip. Many extra supply and ground pins were distributed throughout the pad frame along with extra analog pins for testing, resulting in 235 pins total.

Test structures were put in the lower left area of the chip and had separate supply and ground pins. These included test pixels, different photodiodes, and each amplifier used on the chip. In addition, two extra ADCs are implemented on either side of the array. One has internal analog nodes wired out to pads and is connected to 8 extra pixels. The other ADC has a direct analog voltage input from off chip so the ADC without the pixel can be characterized and debugged. Figure 4.34 shows the layout of the chip.
Figure 4.34: Full chip layout. The chip measures 8x9mm for a 480x480 pixel array.
Chapter 5: Measurement Results

Section 5.1: Testing Configuration and Chip Settings

Figure 5.1: Chip micrograph. This image is 180 degrees rotated compared to the chip layout shown in the previous chapter.

For testing, the chip was packaged in a large 256 pin PGA package (CPG25604) and mounted in a custom socket made with SIP connectors. 3 tunable linear regulators were supplied by a 5V reference that is shared by the FPGA (Spartan 3 XEM3100). These provide the digital and analog supplies as well as the supply for the row select drivers. The FPGA is used to control the exposure time pins on the chip and the
pad enable pins. The master clock is provided by the PLL chip directly from the FPGA board. The data coming out of the imager chip is synchronized in the FPGA using the synchronizing clock from the imager chip. The FPGA converts the 2’s complement signed encoding from -1024 to 1023 to an unsigned encoding from 0 to 2047. Data is only latched into the FPGA when the line valid signal is high. Since the image encoding can only go from -1023 to 1023, the code -1024 is unused. This means 0 is unused when it is sent to the PC from the FPGA, so it is used to encode a falling edge of frame valid, signaling that the next piece of data corresponds to the start of a frame.

The FPGA controls exposure time greater than the inverse of the frame rate by setting the exposure time pins to the enable off code to disable clocks on chip. The extra delay is always triggered by the frame valid signal so that the delay is between frames. The resolution of the delay and therefore exposure time is set by the master clock going into the chip.

The PC communicates with the FPGA through USB 2.0 using Opal Kelly’s FrontPanel software using C++. To achieve real time data transfer and display, the packet size needed to be 8MB for maximum data rate. Thus the FPGA streams data into a FIFO which feeds into the SDRAM chip on the FPGA board and back into another FIFO on the FPGA in order to achieve a large enough packet size for real time data transfer. The developed software could display or save the images in real time and also control exposure time and frame rate.

The Printed Circuit Board was designed so the pins on the FPGA could be directly plugged into the board. In addition, every supply pin on the chip was decoupled to ground using a 1nF and 100nF surface mount capacitor, and a large 10µF capacitor was placed on the board for every supply voltage. Originally the board was also designed with 4 8-bit digital-to-analog converters (DAC) to control various bias pins, but these were later taken off as they were not needed. However, each node driven by the DACs had a 1nF capacitor to ground. The comparator and MDAC buffered voltage references produced on chip were stabilized using 1µF surface mount capacitors on the PCB.

A lens mount was designed and 3D printed using ProE in order to attach a CS-mount on top of the image sensor. It screws directly into the PCB board. The custom SIP socket does not fit very well with the chip, so the lens mount is needed in order to apply pressure to the chip.
Figure 5.2: Testing setup for controlling and interfacing the imager chip with a PC. A shows a block diagram of the system and B shows an image of the PCB board. The red box on the left indicates where the chip is (hidden under the lens mount), and the red box on the right is the FPGA used.

The following settings were found to have the lowest amount of noise. Analog supply was set to 3.3V, digital supply was set to 3.0V, and the row select voltage was set to 2.0V. In addition, the imager was less noisy at 60 fps, but it could still run at 100 fps. The master current bias going into the chip was provided using a divided down version of the 2.0V supply, and the bias used for the top of the resistor ladder to produce the MDAC and comparator voltage references was tied to the analog supply (3.3V). The DDS voltage reference (VCON) was tied to the 1.15V buffered output that was made on chip for MDAC operation.

After tuning, there was still significant noise above expected levels. Signal dependent noise apart from shot noise was found in the form of digital coupling to pixel from digital signals used to control the ADC inside the chip. This was confirmed to be independent of the ADC by looking at noise levels of the ADC at a DC value in high illumination and no illumination and by adjusting the DDS voltage reference (VCON) to provide different offset levels to the ADC in the array during dark illumination. Thus, it must be noise associated with the pixel. Significant digital coupling to the amplifier biases were also found and can be seen in Figure 5.3(A-C). Connecting the amplifier bias nodes to decoupling capacitors originally meant for the DAC outputs reduced the effect of this noise.
Figure 5.3: Digital coupling onto analog nodes. A shows one of pixel pmos biases (pixel_bias) in blue and the digital signal line_valid in yellow in the dark. B shows the same setup during bright illumination. The noise looks periodic because part of the array is not being illuminated due to the limited aperture size of the CS-mount. C shows a zoomed in view of B; it can clearly be seen that the large disturbances happen with the rising and falling edges of line_valid. D shows the analog output of a pixel in yellow; the rectangular portion corresponds to reset and the rest is when the pixel is reading out.

Reducing the frame rate and lowering the digital power supply also reduced this noise. Thus, the image sensor was characterized at 60 fps with a 3.0V digital power supply.

Power consumption was measured with a Keithley 6430 Sub-femto Amp Source Meter in the dark. The 5V supply was disconnected from the regulators and the Keithley supplied the 5V to the corresponding regulator shown in

Table 5.1 and measured the current draw.
Table 5.1: Measured Chip Power Consumption

<table>
<thead>
<tr>
<th>Regulator Voltage</th>
<th>Analog Supply</th>
<th>Digital Supply</th>
<th>Row Select Regulator</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3.3V</td>
<td>3.0V</td>
<td>2.0V</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>73.650mA</td>
<td>33.057mA</td>
<td>145.25µA</td>
</tr>
</tbody>
</table>

Section 5.2: Analog-to-Digital Converter Measurements

A test ADC with its input tied to a pad was used to characterize its performance. It was characterized using a sine wave input with varying amplitudes and a triangle wave. For all tests, the imager was run at 60fps.

Section 5.2.1: ADC Tone Test

The tone test was done using varying amplitude of sine waves at 182.8857 Hz. It was centered at the middle of the ADC range at 1.65V. The frequency was chosen to satisfy coherent sampling [90]. The chosen frequency should satisfy:

\[
f_{\text{opt}} = f_s \left( \frac{I}{M} \right)
\]

(5.1)

Where \(f_{\text{opt}}\) is the input sine wave frequency, \(f_s\) is the sampling frequency, \(J\) is the number of input signal periods in the test sequence and \(M\) is the number of samples in the test sequence. \(J\) should be relatively prime to \(M\). If \(M\) is a power of 2, it will simplify Fourier Transform analysis later.

\[
M = \pi 2^B
\]

(5.2)

Because the imager is running at 60fps, the corresponding sampling frequency of the ADC is now 34.7083µs. \(J\) was chosen to be 13, and \(M\) was chosen to be 2048.

\[
f_{\text{opt}} = \frac{1}{34.7083\mu s} \left( \frac{13}{2^{11}} \right) = 182.8857 Hz
\]

(5.3)
The function generator’s output contained harmonics, so a simple second order low-pass analog filter was put at the output of the function generator before it went into the test ADC. The filter circuit is shown in Figure 5.4. The corner frequency is given by:

\[
f_c = \frac{1}{2\pi \sqrt{R_1C_1R_2C_2}} = \frac{1}{2\pi \sqrt{(200\Omega)(4.7\mu F)(200\Omega)(4.7\mu F)}} \text{Hz} = 169.3138 \text{Hz}
\]  

(5.4)

Figure 5.4: Setup for tone test of the ADC. A simple RC second order low-pass filter was used to reduce the harmonics from the function generator.

The 3dB cutoff frequency for this type of filter is given by:

\[
f_{-3dB} = f_c \sqrt{\frac{1}{2^2 - 1}} = 108.9694 \text{ Hz}
\]  

(5.5)

This was chosen so that first harmonic at 365.7714Hz would be attenuated by a significant amount.

To calculate the tone test results, a Fast Fourier Transform (FFT) was performed on the digitized sine wave. A Hann Window was applied, and the power at each FFT bin was calculated. The first few bins were ignored because of the distortion from using a Hann window.

The Signal-to-Noise Distortion Ratio (SNDR) was calculated using

\[
\text{SNDR} = 10 \times \log_{10}\left(\frac{\sum \text{Power in Sine Frequency bin and two adjacent bins}}{\sum \text{Power in all other bins}}\right)
\]  

(5.6)

Adjacent bins were included because a Hann window was used.

From the SNDR, the Effective Number of Bits (ENOB) can be calculated using
\[ ENOB = \frac{SNDR - 1.76}{6.02} \] (5.7)

The Signal-to-Noise Ratio (SNR) was calculated in a similar way to SNDR, but the power of the bins at the harmonics of the input sine wave are excluded.

\[ SNR = 10 \log_{10} \left( \frac{\sum \text{Power in Sine Frequency bin and two adjacent bins}}{\sum \text{Power in all other bins} - \text{Power in Harmonic bins}} \right) \] (5.8)

The noise of the ADC was calculated by summing the powers of all the bins excluding the harmonic bins and converting the units to bits.

\[ Noise\ Power = \sum \text{Power in all other bins} - \text{Power in Harmonic bins} \] (5.9)

\[ Noise = \sqrt{\left( Noise\ Power \times \left( \frac{\text{Sine\ Wave\ Amplitude}}{2} \right)^2 \right)} \] (5.10)

The Spurious-Free Dynamic Range (SFDR) defined as the ratio of the power at the sine wave frequency to the highest peak in all other bins excluding the two around the sine frequency bin.

\[ SFDR = 10 \log_{10} \left( \frac{\text{Power in Sine Frequency Bin}}{\text{Power of corresponding to highest spurious peak}} \right) \] (5.11)

The results are shown in Figure 5.5. The highest SNDR and ENOB occurs slightly past the resolution of 10 bits implying that the ADC saturation is able to stay linear for a small region before distortions start to degrade the signal.
Figure 5.5: ADC tone test results. A shows the SFDR, SNR and SNDR as a function of the sine wave amplitude, B shows the ENOB as a function of the sine wave peak to peak amplitude, and C shows the Fast Fourier Transform of the amplitude corresponding to the highest ENOB.

Section 5.2.1: Integral and Differential Nonlinearity

To test the Integral Nonlinearity (INL) and Differential Nonlinearity (DNL), a slow triangle wave was passed directly from the function generator to the input of the ADC. The histogram method using a slow triangle wave outlined in [91] was used to calculate INL and DNL.
Figure 5.6: INL and DNL results. A shows the reconstructed ramp using the histogram method from a triangle wave, and B shows the INL and DNL. The maximum DNL was 0.383, and the minimum DNL was -0.9379. The maximum INL was 2.5855 and the minimum INL was -5.999.

The triangle wave used had a frequency of 1Hz and peak to peak amplitude of 2.2V. A single period of the triangle wave was used for analysis. The values of the triangle wave within one period were binned into levels corresponding to the ADC levels. Values outside of the 10 bit range were ignored. DNL was calculated using

\[
DNL = \frac{\text{# counts in bin}}{\text{total # counts}} - 1
\]

To reconstruct the ramp, the values in the bins were sorted, and the indices corresponding to the code transitions were found. A fit line was constructed by drawing a line through the first and last transition points with the y-axis being the codes of the ADC and the x-axis being the sorted data index. The transition points were then mapped to ADC codes using this linear fit and compared to the ideal transition values. INL is defined as the distance from the fit line and the ramp transition points [92].

The ADC performance is summarized in Table 5.2.
### Table 5.2: Summary of Measured ADC Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR (at max ENOB)</td>
<td>51.0355 dB</td>
</tr>
<tr>
<td>SFDR (at max ENOB)</td>
<td>49.8654 dB</td>
</tr>
<tr>
<td>SNDR (at max ENOB)</td>
<td>45.0309 dB</td>
</tr>
<tr>
<td>ENOB (at max ENOB)</td>
<td>7.1879 bits</td>
</tr>
<tr>
<td>Noise (at max ENOB)</td>
<td>1.3687 DN</td>
</tr>
<tr>
<td>Sine Wave peak to peak Amplitude at max ENOB</td>
<td>1100 DN</td>
</tr>
<tr>
<td>INL</td>
<td>+2.5855 / -5.999</td>
</tr>
<tr>
<td>DNL</td>
<td>+0.3830 / -0.9379</td>
</tr>
<tr>
<td>LSB</td>
<td>1.95mV</td>
</tr>
</tbody>
</table>
Section 5.3: Sensitivity Measurements

Section 5.3.1: Optical Setup

To characterize the sensitivity characteristics of the image sensor, different intensities of uniform light were shown on the bare image sensor and measurement parameters were derived according to [71]. Several configurations were tried initially to achieve uniform light intensity at a narrow wavelength. Ideally an integrating sphere would be used to get a very uniform illumination; however, an alternative method had to be used because an integrating sphere was not available. Initially a diffuse LED far away from the sensor was shone directly at the sensor. This was fairly uniform, but spots would appear on the image corresponding to imperfections in the LED. Next, a diffuser (piece of ground glass) was put right after the LED before being shone on the sensor. Though the illumination was now more uniform, the spots still appeared on the image. Next, the same setup was applied in a lens tube, which should collimate the light; however, the spots persisted. With the tools available, the only way to get rid of the spots was to take advantage of diffusive scattering. This was done by reflecting the LED light off of a piece of paper; however, this drastically attenuates the amount of light reaching the sensor. In order to get high enough illumination and high uniformity, a bright light source was needed, and the sensor and light source both needed to be far from the piece of paper. The source used was a Nikon N1-150 white light source. The light intensity was tunable via a knob. It was passed through a 680nm band pass filter with a full width at half maximum (FWHM) of 32nm. 680nm was chosen because there was more power from the light source at higher wavelengths.

A Thorlabs S121C power meter was used to measure the light intensity. This sensor is accurate down to 0.5µW, and has an aperture of 9.5mm (diameter). Since the measured light level needs to go down to at least 100nW per square cm, the light was measured in several spots in order to extrapolate the light level at the sensor. First it was measured close to the light source (facing the light source). This has a much higher irradiance compared to the level at the sensor. Next, the light level was measured directly in front of the image sensor. Since the light intensity was only adjustable with a knob (with no precise markings), the irradiance had to be measured after each image stack was taken. Furthermore, replacing the image sensor with the power meter was not desirable since it would be difficult to put the sensor back in the exact same
place. To get more accurate readings, a point parallel to the image sensor was also taken as well as a point parallel to the measurement in front of the sensor. These two points are parallel to each other as well. These two measurements will be used to get an idea of the attenuation caused by the additional distance from the measurement in front of the sensor to where the sensor is.

**Irradiance Mapping from Light Source to Sensor**

![Graph showing linear relationship between irradiance measured near the light source and in front of the sensor. The equation y = 0.0092x with R² = 0.9958 is shown.]

**Figure 5.7:** Relationship between irradiance measured near the light source and in front of the sensor. This will be used as part of the mapping to extrapolate the irradiance at the image sensor.

For light levels below 1µW/cm² in front of the image sensor, the level in front of the image sensor was extrapolated using the relationship shown in **Figure 5.7**. The light at the image sensor was then taken to be the value in front of the image sensor attenuated by the amount given by the relationship shown in **Figure 5.8**. Thus for low light levels, the irradiance at the image sensor is given by:

\[
I_{\text{sensor}} = \frac{(I_{\text{source}})(0.0092)}{1.0875} \tag{5.13}
\]
Figure 5.8: Relationship between the irradiance at a point parallel to the image sensor and a point parallel to in front of the image sensor to extrapolate the attenuation from the light measured in front of the sensor to what the sensor is seeing.

To confirm that the images had uniform illumination, images were also taken concurrently using a commercial camera (Point Grey GS3-PGE-23S6M-C) that was placed next to the image sensor. All images were taken at 60 fps with an exposure time of 16.667 milliseconds. The percent error from the mean value of the array for the highest illumination used in the measurements is shown in Figure 5.9. All measurements were done in a dark room. A picture of the setup when the irradiance of the light source is being measured is shown in Figure 5.10. All measurements were done at room temperature.
Figure 5.9: Percent Error from the mean value of the array. This image was taken by the commercial Point Grey camera to examine the uniformity of the calibration. The pixel number is shown on the axis, and the pixel size for this camera is 5.86µm.

Figure 5.10: Sensitivity Measurement Setup.
Section 5.3.2: Sensitivity Measurement Results

Sensitivity measurements were analyzed using the methods and equations described in [71]; the document was followed as closely as possible.

For most of the analysis excluding the spatial non-uniformity, defect pixels were excluded from the analysis. Defect pixels were found by doing a non-uniformity correction. An example image is shown in Figure 5.11 with and without the non-uniformity correction. For calibrated images, the defective pixels took on a value equal to the median of a 5x5 array around it.

![A](image1.jpg) ![B](image2.jpg)

Figure 5.11: Non-uniformity Correction applied using 22 points. The raw image is shown in A and the calibrated image is shown in B. Both images are a single frame taken at 60 fps, 16.667ms exposure time. It eliminates most of the Fixed Pattern Noise (FPN) due to mismatch from the sharing pixel structure.

The level to map each pixel to for each light level was determined by drawing a line between the average pixel value for the lowest uniform light level and the average pixel value for the highest uniform light level (before full well). For each uniform light level, each pixel in the array was mapped to the average value of the array using a piecewise linear fit. The slope of each pixel at all the light levels was then examined. If the slope was equal to or less than 0 for the fit between any two light levels, then that means that pixel does not respond properly to light. The median slope value for each light level was found, and any pixel whose slope differed from the median value by more than 6 times the median value was also
deemed to be defective. Pixels whose slope was infinite were also defective. Figure 5.12 shows the
defective pixels found using this method.

Figure 5.12: Defective pixels in the pixel array are shown in black.

Because signal dependent noise was identified that was not shot noise, the conversion gain and
therefore quantum efficiency could not be calculated from the uniform images. Instead an estimate of
conversion gain was used based off of the design. The pixel amplifier should integrate all the charge onto
the feedback capacitor, so the voltage at the output of the pixel is given by

\[ V_{pixel} = \frac{(e^-)1.602 \times 10^{-19}}{C_f} \]

(5.14)

\[ C_f = \frac{10.7 fF}{3} = 3.5667 fF \]

(5.15)

Since the value of a single LSB is known (1.95mV), the output in digital numbers (DN) is

\[ DN = \frac{V_{pixel}}{V_{LSB}} = \frac{(e^-)1.602 \times 10^{-19}}{3.5667 fF \times 10^{-15} \left(\frac{1.95V}{DN} \times 10^{-3}\right)} \]

(5.16)

Since the value of a single LSB is known, then the conversion gain \( K \) is given by:
\[ K = \frac{DN}{e^{-}} = 0.02304 \quad (5.17) \]

This estimated value will be used in the subsequent calculations.

124 frames were taken at each light level. Temporal variance can be calculated for the light level \( y \) using only two frames [71]. For variance calculations, only frames 10 and 11 were used. \( N \) and \( M \) are the number of rows and columns in the array.

\[
\sigma_{y}^{2} = \frac{1}{2NM} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} (y_{10}[m][n] - y_{11}[m][n])^2
\quad (5.18)
\]

The mean value for each illumination was calculated from frames 10 and 11 using a similar method.

\[
\mu_{y} = \frac{1}{2NM} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} (y_{10}[m][n] + y_{11}[m][n])
\quad (5.19)
\]

The Responsivity (R), or sensitivity is defined as the number of DN per photon is given by

\[
R = \frac{\mu_{y} - \mu_{y \text{ dark}}}{\mu_{p}}
\quad (5.20)
\]

It can be calculated by fitting a line when the mean number of photons is plotted against the mean DN values for different illuminations minus the mean DN value for dark level. Since there should be no response beyond the dark level, the intercept of the fit should be zero, and the slope is the Responsivity. Points from 0-70% of the saturation value were used for fitting.
The quantum efficiency $\eta$ is given by

$$\eta = \frac{R}{K} = 21.3\% \quad (5.21)$$

To evaluate the linearity of the sensor response, the fit line used for Responsivity (with the x-axis units now being in $\mu$W/cm$^2$) was compared to the average values. Linearity was established by applying least squares linear regression on points from 5-95% of the saturation level. The fit line is given by:

$$y = a_0 + a_1 H \quad (5.22)$$

Where $a_0$ and $a_1$ are the offset and slope respectively, and $H$ is the light intensity. The relative deviation from the fit line above is

$$\delta_y[i] \% = 100 \left( \frac{\mu_y[i] - \mu_{y\text{ dark}}[i]}{0.9(\mu_{y\text{ sat}} - \mu_{y\text{ dark}})} \right) \quad (5.23)$$

The linear error is then given by

$$LE = \frac{\max(\delta_y) - \min(\delta_y)}{2} \quad (5.24)$$

The calculation and fit were done for raw and calibrated images to show the effects of calibration.
**Figure 5.14:** Linearity of image sensor response. A shows the raw images and B shows the calibrated images. The error bars represent the spatial standard deviation from the average value after temporal averaging within the image. The calibration reduces both the linear error and the spatial standard deviation as the error bars are barely visible in the calibrated curve.

**Figure 5.15:** Photon Transfer Curve shown in log scale for both Noise and Light Intensity. Read noise is 2.7179 DN. Saturation occurs at 886.1168 DN.
The last point in the Photon Transfer Curve represents the last measured point before noise starts decreasing, indicating saturation. Theoretical shot noise is calculated using

\[ \text{Shot Noise} = \sqrt{\text{Light Intensity (photons)} \times \eta \times K} \] (5.25)

Saturation in electrons can be found by dividing the gray value at saturation by the conversion gain or by multiplying the number of photons at saturation by the quantum efficiency.

\[ \mu_{e \text{ sat}} = \eta \mu_{p \text{ sat}} = 38470.3 \text{ e}^- \] (5.26)

The Absolute Sensitivity Threshold is the average number of photons when the Signal-to-Noise ratio is 1, and can be estimated using

\[ \mu_{p \text{ min}} = \frac{1}{\eta} \left( \frac{\sigma_y \text{ dark}}{K} + \frac{1}{2} \right) = 556.3 \text{ photons} \] (5.27)

The Dynamic Range is the ratio of the saturation level divided by the Absolute Sensitivity Threshold expressed in dB.

\[ DR = 20 \times \log_{10} \left( \frac{\mu_{p \text{ sat}}}{\mu_{p \text{ min}}} \right) = 50.2 dB \] (5.28)

The Signal-to-Noise Ratio (SNR) is given by the ratio of the mean gray value and the noise level.

\[ SNR = \frac{\mu_y - \mu_y \text{ dark}}{\sigma_y} \] (5.29)

The theoretical SNR given by just shot noise is

\[ SNR \text{ Shot Noise} = \sqrt{\eta \mu_p} \] (5.30)
Figure 5.16: Signal-to-Noise ratio over different light intensities. The green line shows the theoretical shot noise based off of the quantum efficiency and represents the performance if the sensor was noiseless.

To find the dark current, the mean array values were found when there was no illumination for different exposure times. Exposure times of 25ms, 50ms, 75ms, 100ms, 125ms, 150ms, 175ms, and 200ms were used. A linear fit line was drawn through these points and the slope of the line is the dark current in DN/s. Dividing this number by the conversion gain $K$ gives the dark current in electrons / s.
Spatial non-uniformity was measured using all 124 frames of the dark image and 50% saturation image. Analysis for non-uniformity was done for both raw and calibrated images to demonstrate the effects of calibration. The effect of temporal noise is suppressed by averaging the images in time over 124 frames, and the estimated temporal variance is subtracted off the spatial variance to get an accurate estimate of the spatial variance.

The temporal variance is defined as

$$\sigma_{y \text{ stack}}^2 = \frac{1}{NM} \sum_{n=0}^{N-1} \sum_{m=0}^{M-1} \sigma_s^2[m][n]$$  \hspace{1cm} (5.31)

Where $\sigma_s$ is calculated over L frames using the images s.

$$\sigma_s^2[m][n] = \frac{1}{L-1} \sum_{l=0}^{L-1} \left( s[l][m][n] - \frac{1}{L} \sum_{l=0}^{L-1} s[l][m][n] \right)^2$$  \hspace{1cm} (5.32)

Then the spatial variance is given by

$$s_y^2 = s_{y \text{ measured}}^2 - \frac{\sigma_{y \text{ stack}}^2}{L}$$  \hspace{1cm} (5.33)
The Dark Signal Non-uniformity (DSNU) and Photo Response Non-uniformity (PRNU) are calculated for the dark image and 50% saturation image using

\[
DSNU_{1288} = \frac{s_y^{dark}}{K} \tag{5.34}
\]

\[
PRNU_{1288} = \sqrt{\frac{s_y^{50} - s_y^{dark}}{\mu_y^{50} - \mu_y^{dark}}} \times 100\% \tag{5.35}
\]

The DSNU values were 15.3 DN and 8.7 DN for raw and calibrated images respectively, and the PRNU values were 10.7% and 0.078% for raw and calibrated images respectively.

Horizontal and Vertical Spectrograms were found by first subtracting off the mean of the image to get rid of the DC component. Then the scaled Fourier Transform was done for each row (horizontal) or each column (vertical). For an image \( y \), then each row or column vector \( y[m] \) across the column or row \( n \) has the Fourier Transform

\[
\hat{y}[m][\nu] = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} y[m][n] \times \exp \left( -\frac{2\pi i n \nu}{N} \right) \quad 0 \leq \nu < N \tag{5.36}
\]

The power at each frequency is then averaged over all the row (horizontal) or column (vertical)

\[
p[\nu] = \frac{1}{M} \sum_{m=0}^{M} \hat{y}[m][\nu] \hat{y}^*[m][\nu] - \frac{s_y^{stack^2}}{L} \tag{5.37}
\]

For the spectrogram plots, only the first half of the powers are plotted since it is symmetric.

To calculate the non-whiteness factor \( F \), the spatial variance and white-noise variance need to be calculated. The spatial variance is given by

\[
DSNU: s_y^2 = \frac{1}{N-1} \sum_{\nu=1}^{N} p[\nu] \tag{5.38}
\]

For the dark image, and

\[
PRNU: s_y^2 = \frac{1}{N-15} \sum_{\nu=8}^{N-8} p[\nu] \tag{5.39}
\]

For the 50% saturation image. The white-noise variance was found by taking the median of the power spectrum. The non-whiteness factor is then
Figure 5.18: Vertical and Horizontal Spectrograms for DSNU of raw and calibrated images. A is the raw vertical DSNU spectrogram, B is the vertical calibrated DSNU spectrogram, C is the raw horizontal DSNU spectrogram, and D is the calibrated horizontal DSNU spectrogram. Calibration lowers the white and spikes of the vertical histogram, which should correspond to the FPN.
Figure 5.19: Vertical and Horizontal Spectrograms for PRNU (50% saturation image) of raw and calibrated images. A is the raw vertical PRNU spectrogram, B is the vertical calibrated PRNU spectrogram, C is the raw horizontal PRNU spectrogram, and D is the calibrated horizontal PRNU spectrogram. Calibration lowers the spatial standard deviation.

Histograms and accumulated histograms can be constructed for the DSNU and PRNU to look at the distribution of pixels. The PRNU image was first high passed filtered by subtracting out a 5x5 box filter.

\[ y' = y - R \cdot y \]  
(5.41)
Bins for the histogram were selected by evenly spacing 256 from the minimum to the maximum value in the image. The non-white variance was calculated by subtracting the white-noise component from the total variance. This time instead of finding the median of the row or column FFT, a 2 dimensional FFT was done and the median of the power was taken to be the white component.

The fit line was then given by

\[
p_{\text{normal}}[q] = \frac{y_{\text{max}} - y_{\text{min}}}{Q} * \frac{NM}{\sqrt{2\pi}s_{\text{nw}}} * \exp \left( -\frac{(y[q]^2)}{2s^2_{\text{nw}}} \right)
\]

\[
y[q] = y_{\text{min}} + \frac{q + 0.5}{Q} * (y_{\text{max}} - y_{\text{min}})
\]

\[
R = \begin{bmatrix}
1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1
\end{bmatrix} / 25
\]
Figure 5.20: DSNU Histograms. A shows the raw data histogram, B shows the calibrated data histogram, C shows the raw data accumulated histogram and D shows the calibrated data accumulated histogram. Calibration reduces the deviation from the mean.
Figure 5.21: PRNU Histograms. A shows the raw data histogram, B shows the calibrated data histogram, C shows the raw data accumulated histogram and D shows the calibrated data accumulated histogram. Calibration reduces the deviation drastically.

The imager sensitivity characteristics are summarized in the table below. Fill factor was based off the size of the NWELL in the layout.
<table>
<thead>
<tr>
<th>Sensitivity Parameter</th>
<th>Measurement Result at room temperature, 680nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Gain ((K))</td>
<td>0.023 DN/e(^{-})</td>
</tr>
<tr>
<td>Read Noise</td>
<td>2.7179 DN</td>
</tr>
<tr>
<td>Responsivity ((R))</td>
<td>0.0049066 DN/photon</td>
</tr>
<tr>
<td>Quantum Efficiency ((\eta))</td>
<td>21.3%</td>
</tr>
<tr>
<td>Fill Factor</td>
<td>37.335%</td>
</tr>
<tr>
<td>Linear Error ((\text{Raw}))</td>
<td>1.4734%</td>
</tr>
<tr>
<td>Linear Error ((\text{Calibrated}))</td>
<td>0.18687%</td>
</tr>
<tr>
<td>Max SNR</td>
<td>40.01dB</td>
</tr>
<tr>
<td>Saturation Capacity</td>
<td>38470.3 e(^{-})</td>
</tr>
<tr>
<td>Absolute Sensitivity Threshold</td>
<td>556.21 photons</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>50.2dB</td>
</tr>
<tr>
<td>Dark Current</td>
<td>252.54 DN/s or 10963.8 e(^{-})/s</td>
</tr>
<tr>
<td>DSNU(_{1288})</td>
<td>15.32 DN</td>
</tr>
<tr>
<td>PRNU(_{1288})</td>
<td>10.71%</td>
</tr>
<tr>
<td>Calibrated DSNU(_{1288})</td>
<td>8.69 DN</td>
</tr>
<tr>
<td>Calibrated PRNU(_{1288})</td>
<td>0.078%</td>
</tr>
</tbody>
</table>
### Table 5.4: Comparison of Imager Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>This Work</th>
<th>GS3-PGE-23S6M-C (Sony Pregius IMX174)</th>
<th>TBioCAS 2016 [81]</th>
<th>TBioCAS 2011 [49]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.35 µm 4M2P</td>
<td>0.35 µm 4M2P</td>
<td>0.5 µm 3M2P</td>
<td></td>
</tr>
<tr>
<td>Fill Factor</td>
<td>37.335%</td>
<td></td>
<td>26%</td>
<td>42%</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>10µmx10µm</td>
<td>5.86µmx5.86µm</td>
<td>9.5µmx9.5µm</td>
<td>20.1µmx20.1µm</td>
</tr>
<tr>
<td>Array Size</td>
<td>480x480</td>
<td>1920x1200</td>
<td>144x144</td>
<td>132x124</td>
</tr>
<tr>
<td>Output</td>
<td>10-bits</td>
<td>12-bits</td>
<td>Analog Voltage</td>
<td>Analog Voltage</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>0.023 DN/e</td>
<td></td>
<td>1.961 DN/e</td>
<td></td>
</tr>
<tr>
<td>Read Noise</td>
<td>2.7179 DN</td>
<td>13.3922 DN</td>
<td>1.9mV</td>
<td>0.824mV</td>
</tr>
<tr>
<td>Responsivity (R)</td>
<td>0.0049066 DN/photon, 680nm</td>
<td>1.5098 DN/photon, 525nm</td>
<td>39.5 ( V / (\mu W \cdot cm^2) ) s</td>
<td>16 ( V / (\mu W \cdot cm^2) ) s</td>
</tr>
<tr>
<td>Quantum Efficiency (η)</td>
<td>21.3% (680nm)</td>
<td>77% (525nm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max SNR</td>
<td>40.01dB</td>
<td>45.14dB</td>
<td>49dB</td>
<td>44dB</td>
</tr>
<tr>
<td>Saturation Capacity</td>
<td>38470.3 e</td>
<td>32691 e</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Absolute Sensitivity Threshold</td>
<td>556.21 photons</td>
<td>9.75 photons</td>
<td>90.62 photons</td>
<td>520 photons</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>50.23dB</td>
<td>72.99dB</td>
<td>61dB</td>
<td>48dB</td>
</tr>
<tr>
<td>Power Draw</td>
<td>342.5mW (60 fps)</td>
<td>4.5W</td>
<td>0.6mW (60fps)</td>
<td>2.5mW</td>
</tr>
<tr>
<td>Frame rate</td>
<td>Max 100</td>
<td>10 bit:162,12 bit:128</td>
<td>60</td>
<td>70</td>
</tr>
</tbody>
</table>

The commercial camera outperforms this work in every aspect; it most likely uses a specialized CIS process seeing as it was developed by Sony. Zhang [81] and Murari’s [49] work also generally does better. Murari’s work has a large pixel size and small array size, so it is not suited to this application. Zhang’s work has similar pixel size and uses a similar technology, but has a small array size and no digital output. However, the sensitivity and noise characteristics are much better. This work falls short because the noise is higher than expected likely due to coupling from digital signals. This was likely not an issue for Zhang’s and Murari’s designs because they did not have an ADC on chip. If the noise was near expected levels, the performance should be similar to [81].
Section 5.4: Multiple Exposure Time Functionality

Figure 5.22: Same scene imaged with different exposure times at 100fps. Images have been calibrated.

Multi-exposure capability was functional for both exposure times below the usual exposure time for a given frame rate in a rolling shutter camera and exposure times above. Exposure times below the nominal exposure time for a given frame rate had slightly different FPN. To get rid of this, a different set of uniform images for different irradiances could be taken for that exposure time.

Section 5.5: Other Noise Sources

The read noise is significantly higher than expected, and in addition there is signal dependent noise. Figure 5.23 clearly shows the additional signal dependent noise. To investigate why the read noise is higher and possible sources of the signal dependent noise, the pixel circuit will be analyzed in more detail to look at other possible noise sources.
Figure 5.23: The photon transfer curve plotted with the theoretical shot noise + read noise. Clearly there is signal dependent noise as the measured noise is much higher than if read noise was signal independent.

Section 5.5.1: Shot Noise from Tie-down Diodes

Figure 5.24: Simplified pixel circuit for analyzing the shot noise from tie down diodes
The most obvious signal dependent noise could come from the tie down diodes, which act as photodiodes. The shot noise from the current flowing through the diodes will be analyzed in the circuit shown in Figure 5.24. The impedance for the capacitors will be notated with $Z$. Writing KCL:

\[
\frac{V_{\text{out}} - V_2}{Z_{fb}} = \frac{V_2}{Z_d} + \frac{V_2 - V_1}{Z_{fb}} \quad (5.46)
\]

\[
\frac{V_2 - V_1}{Z_{fb}} = \frac{i_{\text{shot}}}{Z_d} + \frac{V_1 - V_{\text{in}}}{Z_{fb}} \quad (5.47)
\]

\[
\frac{V_1 - V_{\text{in}}}{Z_{fb}} = \frac{V_{\text{in}}}{Z_{pd}} \quad (5.48)
\]

Also from our model of the ideal amplifier, we get

\[-A(V_{\text{in}}) = V_{\text{out}} \quad (5.49)\]

Substituting (5.49) into (5.48)

\[
\frac{V_1 + \frac{V_{\text{out}}}{A}}{Z_{fb}} = -\frac{V_{\text{out}}}{(A)(Z_{pd})} \quad (5.50)
\]

\[
V_1 = -\frac{V_{\text{out}}}{A} \left( \frac{Z_{fb}}{Z_{pd}} + 1 \right) \quad (5.51)
\]

Substituting this and the model of the ideal amplifier into the second equation:

\[
\frac{V_2 + \frac{V_{\text{out}}}{A} \left( \frac{Z_{fb}}{Z_{pd}} + 1 \right)}{Z_{fb}} = \frac{-V_{\text{out}}}{A} \left( \frac{Z_{fb}}{Z_{pd}} + 1 \right) + \frac{-V_{\text{out}}}{A} \left( \frac{Z_{fb}}{Z_{pd}} + 1 \right) + \frac{V_{\text{out}}}{A} \quad (5.52)
\]

\[
V_2 = \frac{V_{\text{out}}}{A} \left( 2 \left( \frac{Z_{fb}}{Z_{pd}} - 1 \right) + \frac{Z_{fb}}{Z_d} \left( \frac{Z_{fb}}{Z_{pd}} - 1 \right) \right) + i_{\text{shot}}Z_{fb} \quad (5.53)
\]

\[
V_2 = -\frac{V_{\text{out}}}{A} \left( 2 \left( \frac{Z_{fb}}{Z_{pd}} + 1 \right) + \frac{Z_{fb}}{Z_d} \left( \frac{Z_{fb}}{Z_{pd}} + 1 \right) - 1 \right) + i_{\text{shot}}Z_{fb} \quad (5.54)
\]

\[
V_2 = -\frac{V_{\text{out}}}{A} \left( 3 \left( \frac{Z_{fb}}{Z_{pd}} \right) + \frac{Z_{fb}}{Z_d} \left( \frac{Z_{fb}}{Z_{pd}} \right) + 1 \right) + i_{\text{shot}}Z_{fb} \quad (5.55)
\]

Rewriting (5.46)

\[
V_{\text{out}} = Z_{fb}i_{\text{shot}} + V_2 \left( \frac{Z_{fb}}{Z_d} + 2 \right) - V_1 \quad (5.56)
\]

Substituting our equation of $V_2$ and $V_1$
\[ V_{out} = Z_{fb}i_{shot} + \left( -\frac{V_{out}}{A} \left( 3 \left( \frac{Z_{fb}}{Z_{pd}} \right) + \frac{Z_{fb}}{Z_{d}} \left( \frac{Z_{fb}}{Z_{pd}} \right) + 1 \right) + i_{shot}Z_{fb} \right) \left( \frac{Z_{fb}}{Z_{d}} + 2 \right) \]

\[ = Z_{fb}i_{shot} + \left( i_{shot}Z_{fb} \right) \left( \frac{Z_{fb}}{Z_{d}} + 2 \right) \]

If \( A \gg 1 \)

\[ V_{out} = Z_{fb}i_{shot} \left( \frac{Z_{fb}}{Z_{d}} + 3 \right) \]

\[ V_{out} = \frac{i_{shot}}{j\omega C_{fb}} \left( \frac{C_{d}}{C_{fb}} + 3 \right) \]

If \( 3C_{fb} \gg C_{d} \)

\[ V_{out} = \frac{3i_{shot}}{j\omega C_{fb}} \]

The noise power is then

\[ V_{out}^2(f) = \frac{9i_{shot}^2}{\omega^2 C_{fb}^2} = \frac{9i_{shot}^2}{4\pi^2 C_{fb}^2} \left( \frac{1}{f^2} \right) \]

The lower end of our bandwidth is limited by the frame rate. Let us use \( 60 \text{Hz} \). The higher end of the bandwidth is limited by the bandwidth of the amplifier, let us use \( 100,000 \).

\[ V_{outRMS}^2 = \frac{9i_{shot}^2}{4\pi^2 C_{fb}^2} \int_{60}^{100k} \frac{1}{f^2} df = \frac{9i_{shot}^2}{4\pi^2 C_{fb}^2} \left( -\frac{1}{100000^2} - \left( -\frac{1}{60^2} \right) \right) \]

\[ V_{outRMS}^2 \approx \frac{9i_{shot}^2}{4\pi^2 C_{fb}^2} 2.68 \times 10^{-4} \]

For \( C_{fb} = 10.7fF \)

\[ V_{outRMS}^2 \approx i_{shot}^2 5.53 \times 10^{23} \]

\[ V_{outRMS} \approx i_{shot} 7.44 \times 10^{11} \]
For reference at the expected light level, the photodiode current is estimated to be around 10fA, or 62422 electrons / sec. If we consider that these tie down diodes receive 10 times lower number of electrons, which is a very generous estimate considering the size of the diode, type of diode, and metal covering the diode, then the shot noise is approximately

\[
\sqrt{ \frac{62422 \text{ electrons}}{\text{sec}}} \approx 79 \frac{\text{electrons}}{\text{sec}} = 12.7 \text{aA}
\]  

(5.67)

This corresponds to an output RMS voltage of

\[
V_{\text{out RMS}} \approx 12.7 \times 10^{-18} \times 7.44 \times 10^{11} = 9.45 \mu V
\]

(5.68)

This is very small compared to the output noise of the amplifier, so we can ignore this noise source at the expected light level. At saturation, the number of electrons is

\[
electrons = 38470.3
\]

(5.69)

Again let’s assume that the tie down diodes receive 10 times less light and therefore ten times less electrons.

\[
\sqrt{ \frac{3847.03 \text{ electrons}}{16.67 \times 10^{-3} \text{ sec}}} \approx 3721 \frac{\text{electrons}}{\text{sec}} = 0.596 \text{fA}
\]

(5.70)

\[
V_{\text{out RMS}} \approx 0.596 \times 10^{-15} \times 7.44 \times 10^{11} = .444 \mu V
\]

(5.71)

Even near the amplifier saturation, the output noise is fairly small compared to the other noise sources.
Figure 5.25: Simplified schematic diagrams for pixel circuit during readout (A). B shows the circuit in A redrawn using the miller effect, and C shows the circuit to be analyzed.

The readout noise from the resistance of the switch will be analyzed next. We want to know the noise at Vin, which is determined by the noise from the amplifier which we know from simulation and the noise of the switch. We can first find the noise from the switch at the input of the amplifier and then add the noise from the amplifier to get the total noise during readout (of the pixel). Writing KCL we get

\[ \frac{V_1}{Z_{pd}} = \frac{V_{in} - (v_r + V_1)}{R} \]  
\[ (5.72) \]

\[ \frac{V_{in}}{Z_{fb}} = -\frac{V_{in} - (v_r + V_1)}{R} \]  
\[ (5.73) \]
Solving for $V_1$ in (5.72) yields

$$V_1 \left( \frac{1}{Z_{pd}} + \frac{1}{R} \right) = \frac{V_{in} - v_r}{R} \quad (5.74)$$

$$V_1 \left( \frac{R + Z_{pd}}{Z_{pd}R} \right) = \frac{V_{in} - v_r}{R} \quad (5.75)$$

$$V_1 = \frac{Z_{pd}(V_{in} - v_r)}{R + Z_{pd}} \quad (5.76)$$

Solving (5.73) for $V_{in}$:

$$\frac{V_{in}}{Z_{fb}} = -\frac{V_{in} - (v_r + V_1)}{R} \quad (5.77)$$

$$V_{in} \left( \frac{1}{Z_{fb}} + \frac{1}{R} \right) = \frac{v_r + V_1}{R} \quad (5.78)$$

$$V_{in} \left( \frac{Z_{fb} + R}{Z_{fb}R} \right) = \frac{v_r + V_1}{R} \quad (5.79)$$

$$V_{in} = \frac{Z_{fb}(v_r + V_1)}{Z_{fb} + R} \quad (5.80)$$

Substituting in $V_1$

$$V_{in} = \frac{Z_{pd}(V_{in} - v_r)}{R + Z_{pd}} \quad (5.81)$$

$$V_{in} = \frac{Z_{fb}v_r}{R + Z_{pd}}$$

$$V_{in}(Z_{fb} + R)(R + Z_{pd}) = Z_{fb}(v_r(R + Z_{pd}) + Z_{pd}(V_{in} - v_r)) \quad (5.82)$$

$$V_{in} \left( (Z_{fb} + R)(R + Z_{pd}) - Z_{fb}Z_{pd} \right) = Z_{fb}v_rR \quad (5.83)$$

$$V_{in} = \frac{Z_{fb}v_rR}{(Z_{fb} + R)(R + Z_{pd}) - Z_{fb}Z_{pd}} \quad (5.84)$$

$$V_{in} = \frac{Z_{fb}v_rR}{Z_{fb}R + Z_{fb}Z_{pd} + R^2 + RZ_{pd} - Z_{fb}Z_{pd}} \quad (5.85)$$
\[ V_{in} = \frac{Z_{fb} v R}{Z_{fb} R + R^2 + R Z_{pd}} \] (5.86)

\[ V_{in} = \frac{Z_{fb} v_r}{Z_{fb} + R + Z_{pd}} \] (5.87)

\[ V_{in} = \frac{v_r}{1 + \frac{R R_{fb} + Z_{pd}}{Z_{fb}}} \] (5.88)

\[ V_{in} = \frac{v_r}{1 + R j \omega C_{fb}(1 + A) + \frac{C_{fb}(1 + A)}{C_{pd}}} \] (5.89)

\[ V_{in}^2(f) = \frac{v_r^2}{R^2 2^2 c_{fb}^2 (1 + A)^2 + \left(1 + \frac{C_{fb}(1 + A)}{C_{pd}}\right)^2} \] (5.90)

\[ V_{in}^2(f) = \frac{v_r^2}{R^2 4 \pi^2 f^2 C_{fb}^2 (1 + A)^2 + \left(1 + \frac{C_{fb}(1 + A)}{C_{pd}}\right)^2} \] (5.91)

Integrating over all frequencies to get the noise:

\[ V_{in}^2 = \int_0^\infty \frac{v_r^2}{R^2 4 \pi^2 f^2 C_{fb}^2 (1 + A)^2 + \left(1 + \frac{C_{fb}(1 + A)}{C_{pd}}\right)^2} df \] (5.92)

\[ V_{in}^2 = v_r^2 \int_0^\infty \frac{1}{R^2 4 \pi^2 C_{fb}^2 (1 + A)^2 + \left(1 + \frac{C_{fb}(1 + A)}{C_{pd}}\right)^2} \frac{df}{f^2 + 1} \] (5.93)

Make the substitution

\[ f^2 = f^2 \frac{R^2 4 \pi^2 C_{fb}^2 (1 + A)^2}{\left(1 + \frac{C_{fb}(1 + A)}{C_{pd}}\right)^2} \] (5.94)

\[ f' = f \frac{R 2 \pi C_{fb}(1 + A)}{\left(1 + \frac{C_{fb}(1 + A)}{C_{pd}}\right)} \] (5.95)

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\[ df' = df \frac{R^2 \pi C_{fb}(1 + A)}{\left( 1 + \frac{C_{fb}(1 + A)}{C_{pd}} \right)} \]

\[ df' \frac{\left( 1 + \frac{C_{fb}(1 + A)}{C_{pd}} \right)}{R^2 \pi C_{fb}(1 + A)} = df \]

\[ V_{in}^2 = v_r^2 \frac{\left( 1 + \frac{C_{fb}(1 + A)}{C_{pd}} \right)}{R^2 \pi C_{fb}(1 + A)} \int_0^\infty \frac{1}{f'^2 + 1} df' \]

We know the noise power of the resistor is:

\[ v_r^2 = 4KTR \]

The integral part is equal to

\[ \int_0^\infty \frac{1}{f'^2 + 1} df' = \frac{\pi}{2} \]

\[ V_{in}^2 = 4KTR \frac{\left( 1 + \frac{C_{fb}(1 + A)}{C_{pd}} \right)}{R^2 \pi C_{fb}(1 + A)} \frac{\pi}{2} \]

\[ V_{in}^2 = KT \frac{\left( 1 + \frac{C_{fb}(1 + A)}{C_{pd}} \right)}{C_{fb}(1 + A)} \]

\[ V_{in}^2 = KT \left( \frac{1}{C_{fb}(1 + A)} + \frac{1}{C_{pd}} \right) \]

If

\[ C_{fb}(1 + A) \gg C_{pd} \text{ or } \frac{1}{C_{fb}(1 + A)} \ll \frac{1}{C_{pd}} \]

\[ V_{in}^2 = \frac{KT}{C_{pd}} \]

The readout noise reduces to KTC noise

From the layout extraction, the photodiode capacitance is 19.7fF. For room temperature of 300K,

\[ V_{in}^2 = \frac{KT}{C_{pd}} = \frac{(1.38)(10^{-23})(300K)}{(19.7fF)(10^{-15})} = 210.15nV^2 \]
Section 5.5.3: Pixel Reset Noise

![Diagram of pixel circuit](image)

**Figure 5.26:** Schematic of simplified pixel circuit during reset phase. A shows the circuit and B shows the circuit used for noise analysis. \( C_{pd} \) is the photodiode capacitance, \( C_{fd} \) is the floating diffusion capacitance, \( C_{fb} \) is the feedback capacitance, and \( C_{load} \) is the load capacitance on the amplifier. The noise of the amplifier is represented by \( v_a \) and we know the value from simulation. The noise from the resistors are represented by \( v_r \) and \( v_{r2} \).

We would like to know the noise at the photodiode, represented by \( V_1 \).

Writing KCL

\[
\frac{V_1}{Z_{pd}} = \frac{V_{in} - (V_1 + v_r)}{R} \quad (5.107)
\]

\[
\frac{V_{out} - (V_{in} + v_{r2})}{R_2} + \frac{V_{out} - V_{in}}{Z_{fb}} - \frac{V_{in} - (V_1 + v_r)}{Z_{fd}} = \frac{V_{in} - (V_1 + v_r)}{R} \quad (5.108)
\]

And from the amplifier,

\[
V_{out} = -A(V_{in} + v_d) \quad (5.109)
\]

Substituting this into (5.108)
\[-\frac{A(V_{in} + v_a) - (V_{in} + v_{r2})}{R_2} + \frac{-A(V_{in} + v_a) - V_{in}}{Z_{fb}} = \frac{V_{in} - (V_1 + v_r)}{R}\]  \hspace{1cm} (5.110)

\[V_{in}\left(\frac{1 + A}{Z_{fb}} + \frac{1 + A}{R_2} + \frac{1}{Z_{fd}}\right) - \frac{v_r}{R} + A\nu_a\left(\frac{1}{R_2} + \frac{1}{Z_{fb}}\right) + \frac{v_{r2}}{R_2} = V_1 \hspace{1cm} (5.111)\]

To simplify things a little bit, we'll assume \(A \gg 1\)

\[V_{in}\left(\frac{1}{R} + \frac{1}{Z_{fb}} + \frac{1}{R_2} + \frac{1}{Z_{fd}}\right) - \frac{v_r}{R} + A\nu_a\left(\frac{1}{R_2} + \frac{1}{Z_{fb}}\right) + \frac{v_{r2}}{R_2} = V_1 \hspace{1cm} (5.112)\]

\[V_{in}\left(\frac{Z_{fd}Z_{fb}R_2 + A(RZ_{fd})(R_2 + Z_{fb}) + Z_{fb}R_2R}{Z_{fd}Z_{fb}R_2R}\right) = \frac{V_1}{R} + \frac{v_r}{R} - A\nu_a\left(\frac{Z_{fb} + R_2}{R_2Z_{fb}}\right) - \frac{v_{r2}}{R_2} \hspace{1cm} (5.113)\]

\[V_{in} = \frac{Z_{fb}R_2}{A(R + Z_{fb})}\left(\frac{V_1}{R} + \frac{v_r}{R} - A\nu_a\left(\frac{Z_{fb} + R_2}{R_2Z_{fb}}\right) - \frac{v_{r2}}{R_2}\right) \hspace{1cm} (5.114)\]

Since \(A\) is large and \(R\) and \(R_2\) are of the same magnitude,

\[V_{in} = \frac{Z_{fb}R_2}{A(R + Z_{fb})}\left(\frac{V_1}{R} + \frac{v_r}{R} - A\nu_a\left(\frac{Z_{fb} + R_2}{R_2Z_{fb}}\right) - \frac{v_{r2}}{R_2}\right) \hspace{1cm} (5.115)\]

\[V_{in} = \frac{Z_{fb}R_2(V_1 + v_r)}{A(R)(R_2 + Z_{fb})} - \frac{v_a - \frac{Z_{fb}v_{r2}}{AR_2(R_2 + Z_{fb})}}{A} \hspace{1cm} (5.116)\]

\[V_{in} = \frac{1}{(A)(R_2 + Z_{fb})}\left(\frac{Z_{fb}R_2(V_1 + v_r)}{R} - Z_{fb}v_{r2}\right) - \frac{v_a}{A} \hspace{1cm} (5.117)\]

Substituting this back into (5.107):

\[\frac{V_1}{Z_{pd}} = \frac{1}{(A)(R_2 + Z_{fb})}\left(\frac{Z_{fb}R_2(V_1 + v_r)}{R} - Z_{fb}v_{r2}\right) - \frac{v_a}{A} - (V_1 + v_r) \hspace{1cm} (5.118)\]

\[V_1\left(\frac{R}{Z_{pd}} + 1 - \frac{Z_{fb}R_2(V_1)}{A(R_2 + Z_{fb})}\right) \hspace{1cm} (5.119)\]

\[= \frac{1}{(A)(R_2 + Z_{fb})}\left(\frac{Z_{fb}R_2(v_r)}{R} - Z_{fb}v_{r2}\right) - \frac{v_a}{A} - v_r \hspace{1cm} (5.119)\]

Since \(A\) is large, the ratio divided by \(A\) on the left side is much smaller than one.
\[ V_1 \left( \frac{R + Z_{pd}}{Z_{pd}} \right) = \left( \frac{1}{A(R_2 + Z_{f_b})} \left( \frac{Z_{f_b}R_2(v_r)}{R} - Z_{f_b}v_r \right) \right) - (v_a + v_r) \]  
(5.120)

The part being divided by \( A \) is much smaller than the magnitude of \( v_r \) if \( A \) is large.

\[ V_1 = -\frac{(v_a + v_r)}{R} \]  
(5.121)

\[ V_1 = -\frac{(v_a + v_r)}{R(j\omega C_{pd}) + 1} \]  
(5.122)

Now if we look at the power:

\[ V_1^2(f) = \frac{(v_a + v_r)^2}{R^2\omega^2C_{pd}^2 + 1} \]  
(5.123)

Since the noise sources are independent

\[ V_1^2(f) = \frac{v_a^2 + v_r^2}{R^24\pi^2f^2C_{pd}^2 + 1} \]  
(5.124)

\[ V_1^2 = \int_0^\infty \frac{v_a^2 + v_r^2}{f^2 + 1} df \]  
(5.125)

\[ f' = R^24\pi^2f^2C_{pd}^2 \]  
(5.126)

\[ df' = 2\pi RC_{pd} df \]  
(5.127)

\[ df = \frac{df'}{2\pi RC_{pd}} \]  
(5.128)

\[ V_1^2 = \int_0^\infty \frac{f'}{f^2 + 1} \cdot \frac{1}{2\pi RC_{pd}} df' \]  
(5.129)

\[ V_1^2 = \frac{v_a^2}{2\pi RC_{pd}} \int_0^\infty \frac{1}{f^2 + 1} df' + \frac{1}{2\pi RC_{pd}} \int_0^\infty \frac{v_a^2}{f^2 + 1} df' \]  
(5.130)

\[ V_1^2 = \frac{4KTR}{2\pi RC_{pd}} \left( \frac{\pi}{2} \right) + \frac{1}{2\pi RC_{pd}} \int_0^\infty \frac{v_a^2}{f^2 + 1} df' \]  
(5.131)

\[ V_1^2 = \frac{KT}{C_{pd}} \int_0^\infty \frac{v_a^2}{f^2 + 1} df' \]  
(5.132)
For the amplifier’s contribution, we will need to change the limits of the integral. The higher end of the integral will be changed to the bandwidth of the amplifier and the lower end of the integral will be changed to the frame rate since DDS should cancel frequencies below that.

\[
V_1^2 = \frac{KT}{C_{pd}} + \frac{1}{2\pi RC_{pd}} \int_{60}^{10^6} \frac{v_{na}^2}{f^2 + 1} df
\]  

(5.133)

For \(C_{pd} = 19.7\text{fF}, R = 5\text{kohm},\) the integral was calculated numerically to get:

\[
V_1^2 = 2.1015 \times 10^{-7}V^2 + 1.9090 \times 10^{-4}V^2 = 1.9111 \times 10^{-4}V^2
\]  

(5.134)

\[
V_{\text{rms}} = 13.8mV
\]  

(5.135)

This noise is much higher than the read noise, so presumably the DDS cancels out a good portion of the reset noise.

The shot noise from the tie-down diodes showed a small signal dependent noise; the readout noise and reset noise did not show signal dependent noise, but could account for some of the high read noise; however, because DDS cancels part of the noise, it is not clear how much it contributes. The large amount of signal dependent noise observed can only be attributed to the scoped signal dependent noise on the pixel biases shown in Figure 5.3. Based on scoping the subsequent stage the pixel connects to (DDS), the noise does not seem to be back propagating from there. The only other ways the digital signals could be propagating into the bias nodes is through the ground or analog supply. Since these are separately wired in the chip, it could only be through the substrate for ground or through the ESD protection diodes, which are tied to digital ground and digital supply. Of course, it could also be coupling from off chip through the PCB.
Chapter 6: Discussion

A sensitive CMOS image sensor optimized for low light retinal imaging was presented. The design featured a CTIA pixel design with additional sharing to accommodate a large minimum capacitor value. The sharing structure will allow for design of CTIA pixel designs with very low feedback capacitor values, especially in processes which allow smaller minimum sized capacitors. In addition, parallel column ADCs using multi-bit per stage digitization were implemented on chip. This algorithm simplified the design of the amplifiers by removing the need for gain correction and fully differential amplifiers. Because the gain requirements were lower, fully differential amplifiers were not needed to cancel the effects of charge injection. Programmable exposure times for rolling shutter were also implemented in this design. The chip was a fully functional first prototype, but it had higher noise than expected. This is likely due to coupling from internal digital signals through the ground and supply to sensitive analog biases.

Future iterations of this design could be improved in several ways. Firstly, moving to a process optimized for imagers would increase the amount of photons collected and reduce noise. These processes use special coatings to increase quantum efficiency and are optimized to reduce dark current and photodiode noise. In addition, some of these processes use back-illumination, which gives the pixel 100% fill factor. Depending on the wavelength of operation, this should increase the signal by four to five times. Secondly, a future design should incorporate more careful layout of the pixel, using specialized software to simulate the pinned photodiode to make sure the energy profile is smooth so that all electrons are transferred to the floating diffusion node. Thirdly, if a sharing design is still used, then the TX signals (which I have called row select signals in this thesis), should be pulsed; if the photodiode is designed well then all the charge will go into the floating diffusion so the transistor does not need to stay on [93]. This will eliminate the fixed pattern noise from clock feed-through, and will also allow the transistor at the photodiode to be overdriven. Finally, the analog circuits in the pixel should be more carefully isolated from the other circuitry, and decoupling capacitors should be placed between the biases and ground / supply throughout the chip.

The signal dependent digital coupling is thought to be because of additional current draw from leaky transistors of the digital circuitry under light. The digital power consumption goes up with light level
(from 33mA to 38mA), so the additional power draw could account for the increased noise on the analog bias lines.

The high INL in the ADC is likely due to imperfectly spaced biases generated from an on-chip resistor ladder. In the future, it might be better to supply these voltages from off-chip or use a more accurate structure to generate the voltage references. In this design though, the performance of the ADC was not the limiting factor.
References:


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Curriculum Vitae

Chun-Ming Ernest So was born in Sarnia, Canada in 1991. He graduated from Johns Hopkins University with a B.S. in Biomedical Engineering in 2014 and joined the M.S.E. program in Biomedical Engineering at Johns Hopkins University in the summer of 2014. During his undergraduate studies, he was named a Bloomberg scholar, received the Wye Scholarship and the Richard J. Johns award. Prior to the M.S.E. program, he conducted research on water interfaces with Dr. Gerald Pollack, department of Bioengineering at the University of Washington, and research on modeling biological control systems with Dr. Pablo Iglesias, department of Electrical & Computer Engineering at Johns Hopkins University. During the MSE program, he conducted research as part of the Neuroengineering and Optical Instrumentation group under Dr. Nitish Thakor.

Ernest’s research interests include analog VLSI circuit design for image sensors, data converters and wireless systems. Starting in September 2016, Ernest will be starting doctoral studies at Stanford University in Electrical Engineering.